MediaTek CorePilot™

Heterogeneous Multi-Processing Technology

Delivering extreme compute performance with maximum power efficiency

In July 2013, MediaTek delivered the industry's first mobile system on a chip with Heterogeneous Multi-Processing. The MT8135 chipset for Android tablets features CorePilot technology that maximizes performance and power saving with interactive power management, adaptive thermal management and advanced scheduler algorithms.

Table of Contents

ARM big.LITTLE Architecture 2
big.LITTLE Implementation Models 3
Cluster Migration 3
CPU Migration 3
Heterogeneous Multi-Processing 4
MediaTek CorePilot Heterogeneous Multi-Processing Technology 4
Interactive Power Management 6
Adaptive Thermal Management 6
Scheduler Algorithms 6
The MediaTek HMP Scheduler 6
The RT Scheduler 7
Task Scheduling & Performance 8
CPU-Intensive Benchmarks 8
Web Browsing 9
Task Scheduling & Power Efficiency 9
SUMMARY 11

MediaTek CorePilot™

Heterogeneous Multi-Processing Technology

ARM big.LITTLE Architecture

ARM brought heterogeneous computing to mobile System on a Chip (SoC) designers with its big.LITTLE™ architecture. ARM big.LITTLE combines high-performance 'big' CPUs with energy efficient 'LITTLE' CPUs on the same SoC to reduce energy consumption (and hence preserve battery power), while still delivering peak performance.

Since both CPUs are architecturally compatible, workloads can be allocated to each CPU, on demand, to suit performance needs. High intensity tasks such as games are allocated to the 'big' CPUs, for example, while less demanding tasks such as email and audio playback are allocated to the 'LITTLE' CPUs. The load balancing happens quickly enough to be completely transparent to the user and can reduce energy consumption by up to 70% for common tasks.

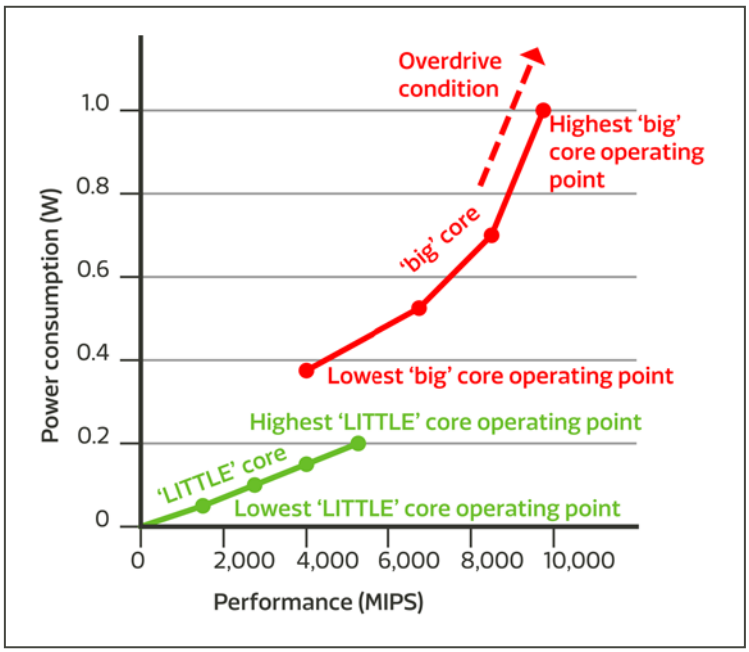

Figure 1: Asymmetric computing with the ARM big.LITTLE architecture

'big' CPU – Performance Driven	'LITTLE' CPU – Energy Efficient
High performance	Moderate performance
High power-consumption	Low power-consumption
Ideal for compute-intensive tasks	Ideal for routine tasks

Table 1: ARM big.LITTLE CPU comparison

big.LITTLE Implementation Models

There are three different software models for implementing heterogeneous computing with the ARM big.LITTLE architecture: Cluster Migration, CPU Migration and Heterogeneous Multi-Processing.

- Cluster Migration

  Cluster Migration groups 'big' and 'LITTLE' CPUs into two clusters and shifts tasks between the two, as required. Only one cluster can be active at a time.

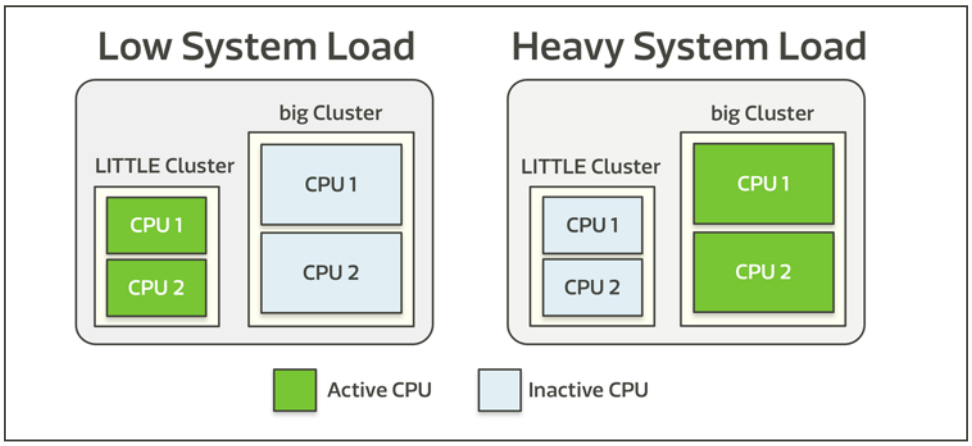

Figure 2: The Cluster migration model

- CPU Migration

  CPU Migration groups each 'big' and 'LITTLE' CPU into a pair, but while a task can be allocated to one or more of these pairs, only one CPU in each pair can be active at a time.

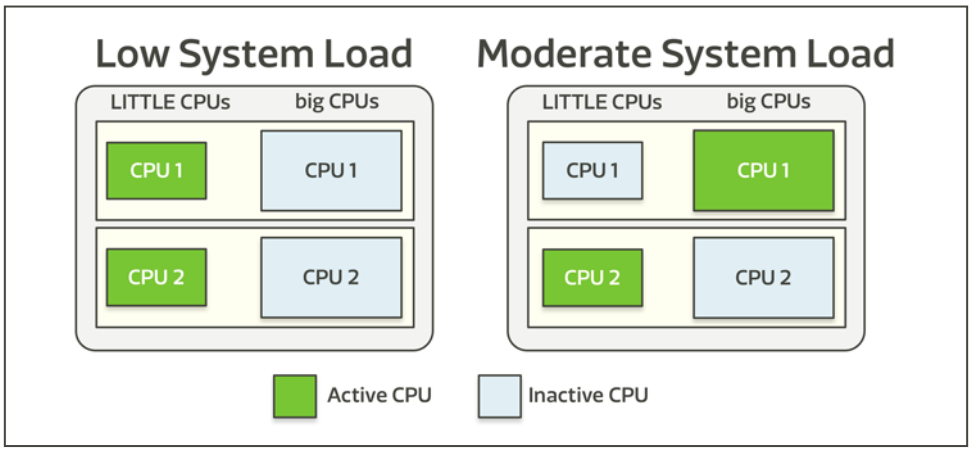

Figure 3: The CPU migration model

- Heterogeneous Multi-Processing

  Heterogeneous multi-processing removes all limitations and allows a task to be allocated to any combination of 'big' and 'LITTLE' CPUs. Heterogeneous multi-processing is extremely flexible and inherently superior to cluster migration and CPU migration, but performance and energy consumption are highly dependent on the SoC's task scheduler.

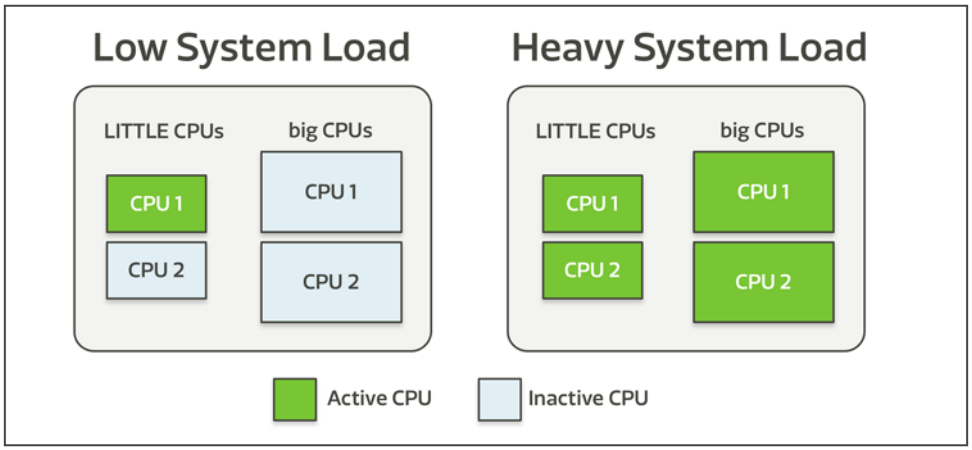

Figure 4: The Heterogeneous multi-processing model

	Cluster Migration	CPU Migration	Heterogeneous Multi-Processing
Switching Granularity	Cluster – low flexibility	CPU – medium flexibility	Unrestricted – high flexibility
Maximum Performance	Medium: 2x 'big'	Medium: 2x 'big'	High: 2x 'big' + 2x 'LITTLE'
Average Power Saving	Low – coarse granularity	Medium	High – fine granularity

Table 2: Comparison of different heterogeneous computing models

MediaTek CorePilot Heterogeneous Multi-Processing Technology

MediaTek is a leader in heterogeneous computing and is actively shaping its future as a founder member of the Heterogeneous System Architecture Foundation (www.hsafoundation.com), a not-for-profit consortium of SoC and software vendors, OEMs, and academia. In July 2013, MediaTek also delivered the industry's first mobile SoC to feature heterogeneous multi-processing (HMP) — the MT8135 chipset with CorePilot technology for Android tablets.

Based on open-source HMP technology derived from Linaro (www.linaro.org), CorePilot maximizes the performance and power-saving potential of heterogeneous computing with interactive power management, adaptive thermal management and advanced scheduler algorithms.

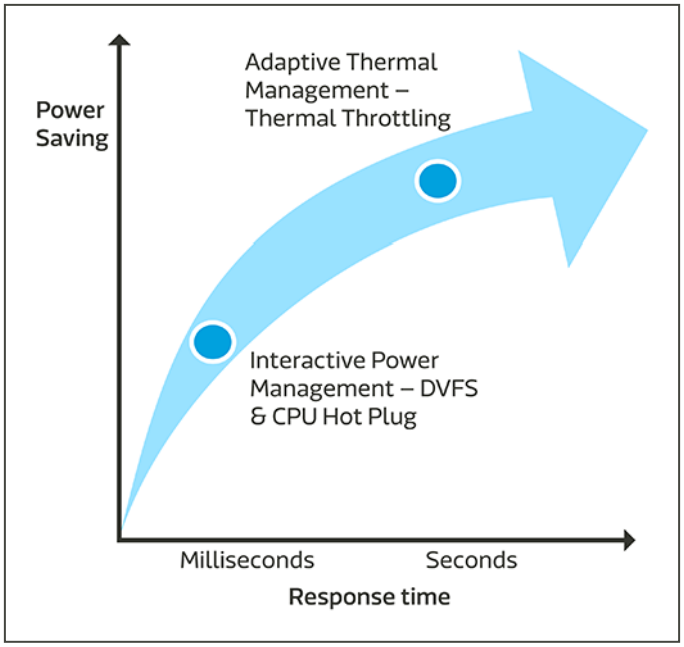

Figure 5: Power-efficiency methods

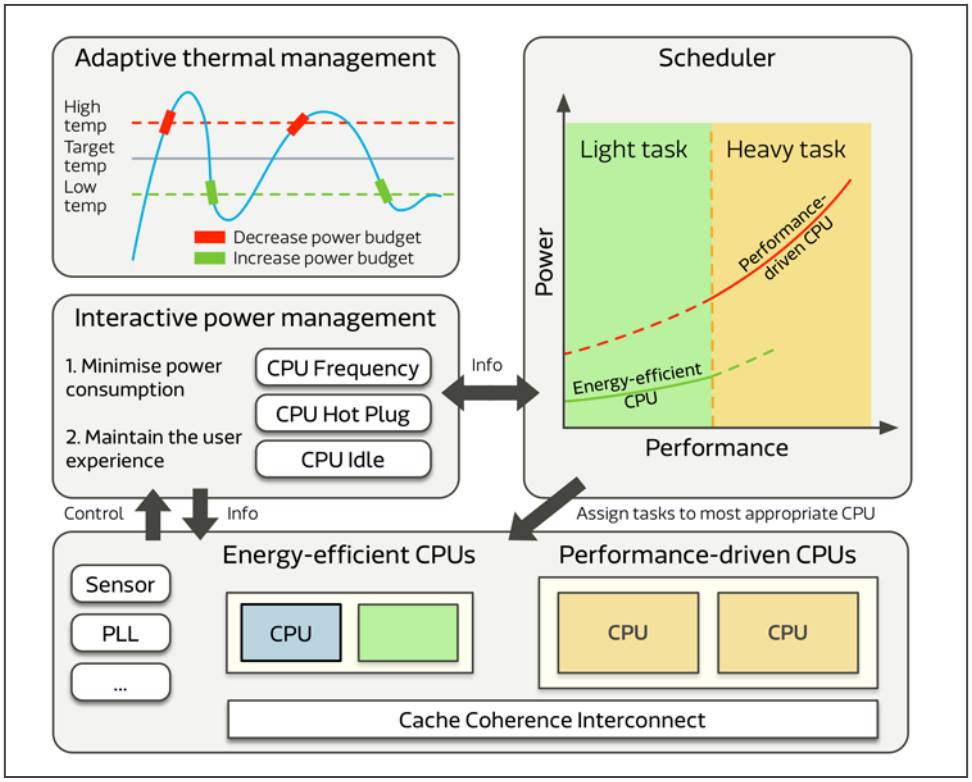

Figure 6: MediaTek CorePilot overview

1. Interactive Power Management

CorePilot's Interactive Power Manager reduces the amount of power and heat generated by CPU via two main modules. The Dynamic Voltage and Frequency Scaling module automatically adjusts the frequency and voltage of CPUs on the fly, while the CPU Hot Plug module switches CPUs on and off on demand.

Dynamic Voltage & Frequency Scaling	Traditional symmetric multi-processors apply a unified Dynamic Voltage and Frequency Scaling (DVFS) policy to all CPUs. CorePilot's Interactive Power Management applies different DVFS policies to 'big' and 'LITTLE' cores to maximize power and thermal efficiency.
CPU Hot Plug	Interactive Power Management monitors CPU load and seamlessly switches cores on or off to save power or to increase performance. CPUs can also be switched off with non-CPU-bound tasks to reduce power consumption.

Table 3: Key components of Interactive Power Management

2. Adaptive Thermal Management

The thermal limits of a mobile device can be exceeded when its CPU or GPU runs at peak performance. This, in turn, can be detrimental to the user experience. Adaptive Thermal Management (ATM) addresses this by monitoring device temperatures and dynamically adjusting the power budget to keep them within a specified range, while minimising the impact on performance. Compared with traditional dynamic power management designs with fixed temperature points for thermal throttling, ATM can achieve a 10% performance increase.

3. Scheduler Algorithms

Performance is the usual goal for operating system scheduling and technology has evolved over time accordingly. With Symmetric Multi-Processing (SMP), the Completely Fair Scheduler (CFS) is currently the most common scheduling algorithm and it distributes the workload equally among CPU cores.

With Heterogeneous Multi-Processing, however, CFS can result in performance degradation, since tasks are not efficiently matched to CPU core capabilities. MediaTek CorePilot, on the other hand, delivers a true heterogeneous compute model by using a scheduling algorithm that assigns tasks to two different schedulers, according to their priority — the Heterogeneous Multi-Processing (HMP) scheduler and Real-Time (RT) scheduler.

- The MediaTek HMP Scheduler

  The HMP scheduler is responsible for assigning normal-priority tasks to the big.LITTLE CPU clusters and performs four main functions.

Load tracking	By tracking the status of each task, the HMP scheduler determines which task is heavy and which task is relatively light.
CPU Capacity Estimation	The HMP Scheduler is aware of the available compute capacity of each processor in the big.LITTLE clusters, and so is able to make the most appropriate scheduling decisions.
Intelligent Load-Balancing	Load tracking and CPU capacity estimation are used in concert for rapid load balancing – assigning and reassigning tasks to performance-driven or energy-efficient CPUs, as required.
Task Packing	The HMP scheduler consolidates as many light-load tasks as possible and matches them to the most appropriate CPUs. CPUs without active tasks can then be switched off via CPU Hot Plug, or put into an idle state.

Table 4: Key components of the MediaTek HMP scheduler

- The RT Scheduler

The RT scheduler assigns high-priority real-time tasks that require a fast CPU response to the big.LITTLE cluster. The RT scheduler has priority over the HMP scheduler and MediaTek has further modified its design so that the highest priority tasks are assigned to performance-driven CPUs. Lesser priority real-time tasks are then assigned to other available CPUs.

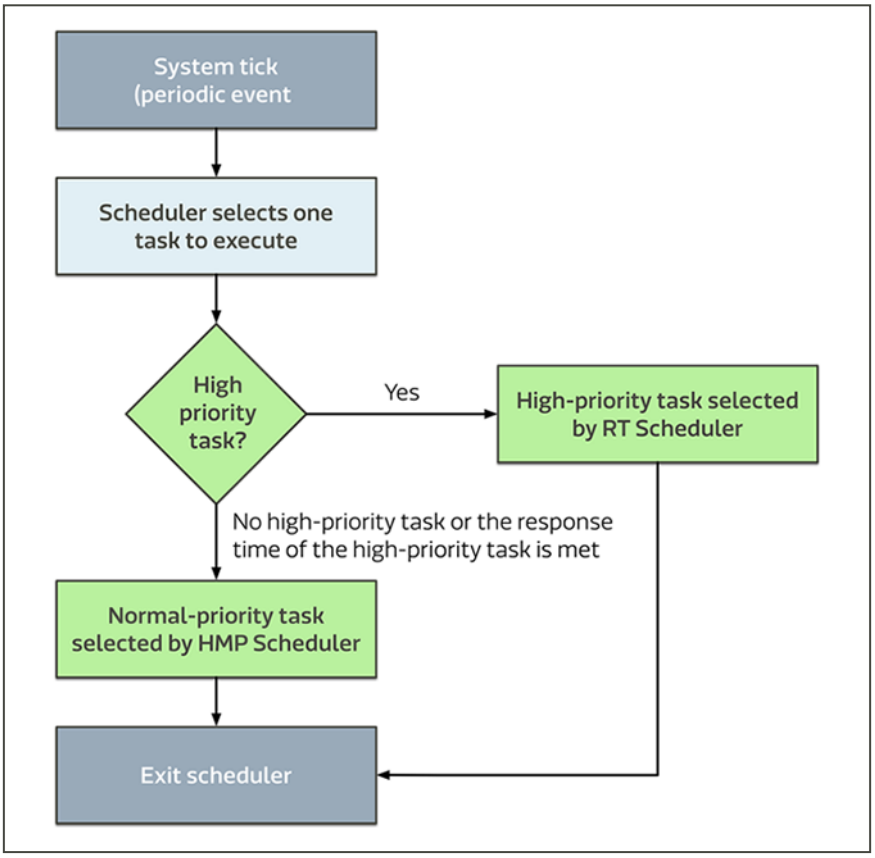

Figure 7: Process flow for the HMP and RT schedulers

Task Scheduling & Performance

Together, CorePilot's HMP and RT schedulers give software simultaneous access to all processors in the big.LITTLE clusters, and tasks are assigned selectively in real-time to strategically manage resources and increase power efficiency. The following real-world examples illustrate the effectiveness of CorePilot with regard to performance.

CPU-Intensive Benchmarks

With a CPU-intensive benchmark such as Antutu v3.3.2 (www.antutu.com), CorePilot spreads the load by assigning one task to each CPU core. The screenshot below, captured using the ARM Development Studio 5 (DS-5) application, shows this in action, with a full load on each core.

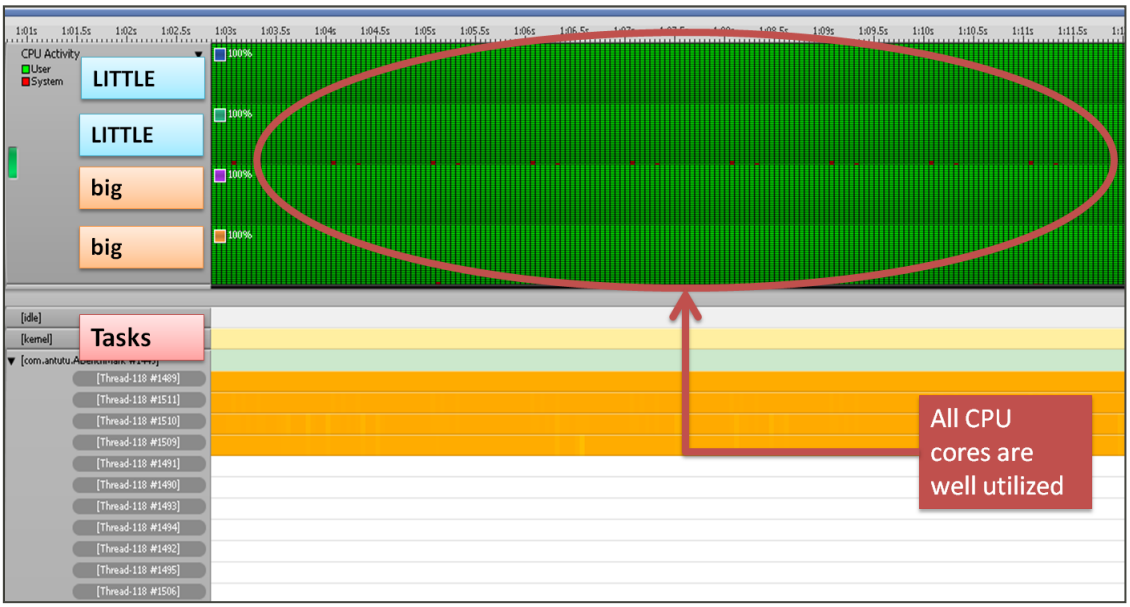

Figure 8: Scheduling on the MT8135 SoC with the Antutu benchmark (data profiled by ARM DS5)

The Linpack (www.netlib.org/benchmark/hpl) and Vellamo (www.quicinc.com/vellamo) benchmarks also clearly illustrate the performance difference between the standard SMP CFS scheduler and the CorePilot HMP scheduler. The benchmarks were run on the MediaTek MT8135 big.LITTLE heterogeneous computing platform.

Linpack is a multi-threaded benchmark and the number of test tasks equals the number of CPU cores. Both the CFS and CorePilot scheduler assign one task to one CPU core, but since CorePilot is aware of the computing capability of each CPU, it can assign the heavy tasks to the performance-driven CPU first, with the remainder assigned to the energy-efficient CPU.

Vellamo ('Metal Chapter') is a single-threaded benchmark. The standard CFS scheduler assigns the benchmark task to the performance-driven or energy-efficient CPU on a random basis, but CorePilot always assigns the task to the performance-driven CPU.

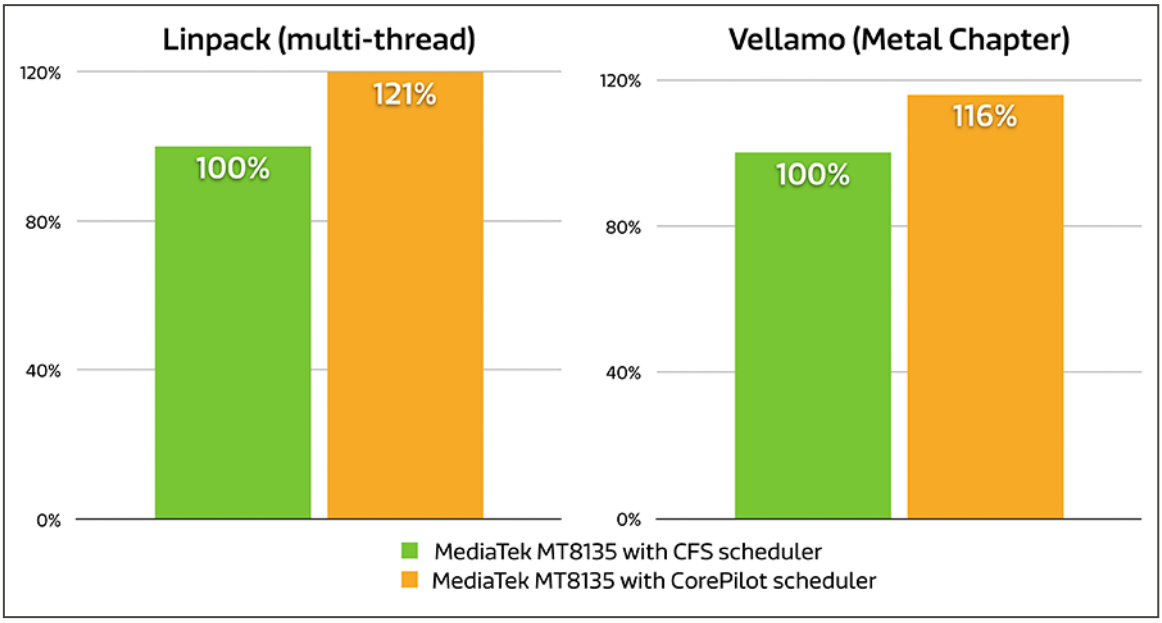

Figure 9: MT8135 benchmark performance comparison

Web Browsing

Web browsing involves a mix of heavy and light tasks, so the CorePilot scheduler assigns tasks to performance-driven or energy-efficient CPUs accordingly. The screenshot below, captured using the ARM Development Studio 5 (DS-5) application, shows this in action.

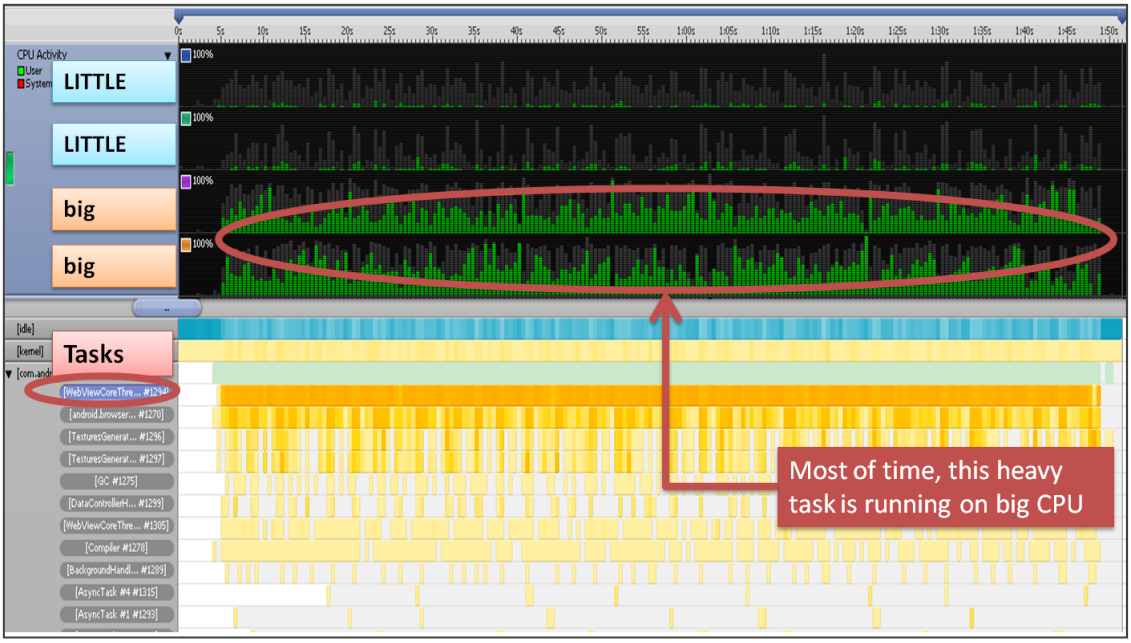

Figure 10: Web browsing on the MT8135 SoC (data profiled by ARM DS5)

Task Scheduling & Power Efficiency

CorePilot's Interactive Power Management not only limits CPU resources for power-efficient performance with light task loads, but also dynamically adjusts the CPU frequency to handle

heavier loads. Figure 11 shows the difference in power consumption between two otherwise identical platforms — the MediaTek MT8135 with an unmodified CFS scheduler and the MT8135 with CorePilot — running the Antutu (www.antutu.com) and Quadrant (www.aurorasoftworks.com) benchmarks.

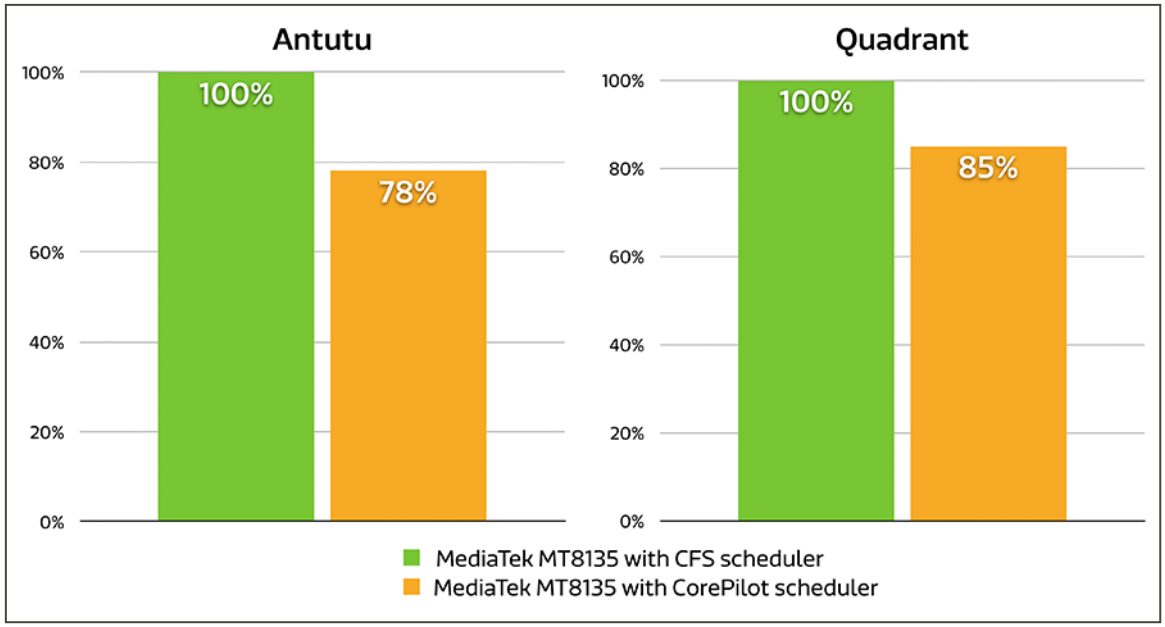

Figure 11: MT8135 energy consumption comparison with benchmarks

Figures 12 and 13 show the difference in energy consumption between the standard ARM Cortex A-15 SMP quad-core platform with CFS and the MediaTek MT8135 HMP platform with CorePilot. CorePilot's interactive power management and adaptive thermal management help reduce energy consumption considerably with both benchmarks and real-world tasks such as multimedia playback. Note that the ARM Cortex A-15 quad-core energy consumption figures are extrapolated from dual-core data.

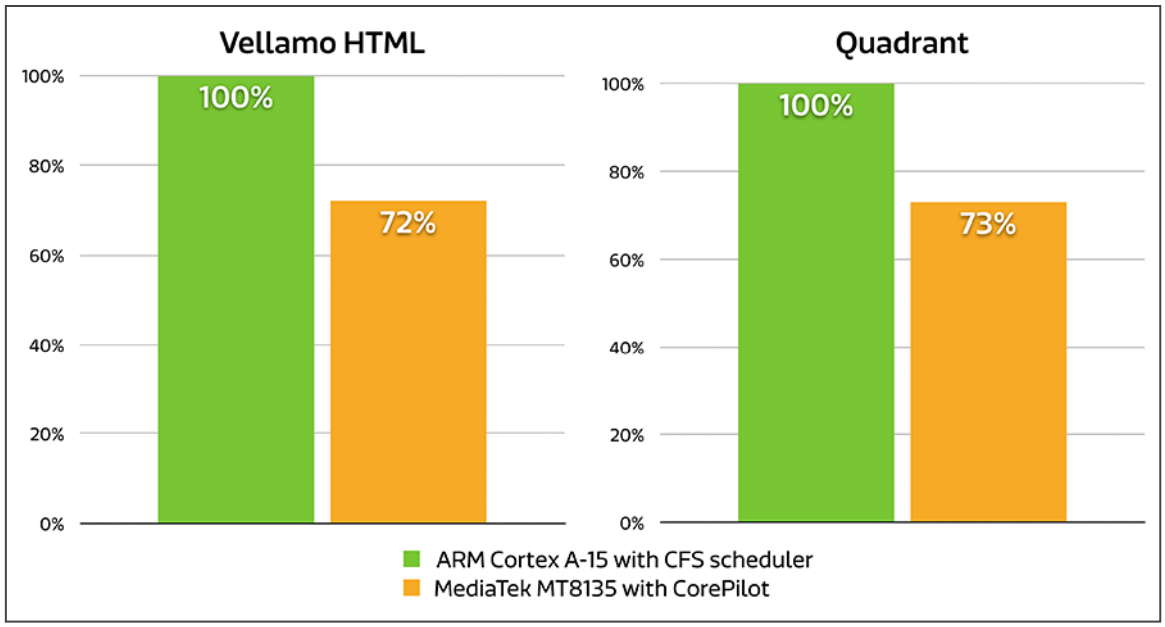

Figure 12: ARM Cortex A15 & MT8135 energy consumption comparison with benchmarks

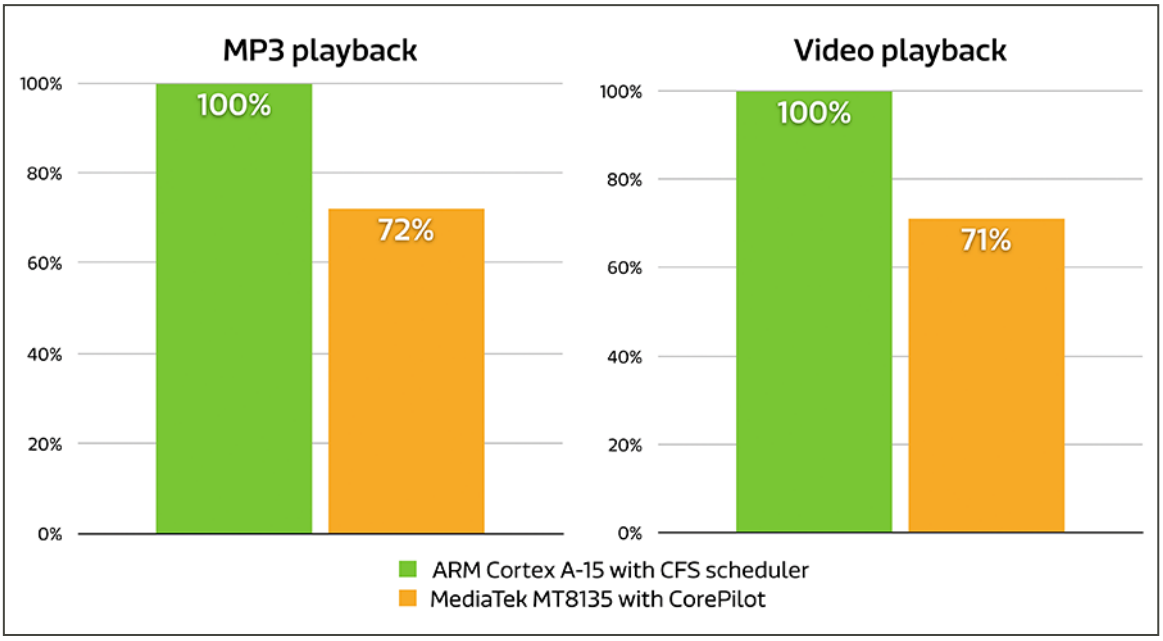

Figure 13: ARM Cortex A15 & MT8135 energy consumption comparison with multimedia playback

SUMMARY

- Mobile SoCs have a limited power consumption budget.
- With ARM big.LITTLE, SoC platforms are capable of asymmetric computing where by tasks can be allocated to CPU cores in line with their processing needs.
- From the three available software models for configuring big.LITTLE SoC platforms, Heterogeneous Multi-Processing offers the best performance.
- MediaTek CorePilot technology is designed deliver the maximum compute performance from big.LITTLE mobile SoC platforms with low power consumption.
- The MediaTek CorePilot MT8135 chipset for Android is the industry's first Heterogeneous Multi-Processing implementation.
- MediaTek leads in the heterogeneous computing space and will release further CorePilot innovations in 2014.