MT6691 2.4MHz 3A ACOT® Step-Down Converter with I²C Interface Datasheet

Version: **1.5**
Release date: **2021-09-01**

Version History

Version	Date	Description
0.1	2017-12-07	Initial draft
1.0	2018-02-12	Top Marking Definition : P10 -Updated marking code Recommended Operating Range : p14 -Modified junction temperature range Electrical Characteristics : P15, P16 -Modified ambient condition -Modified test condition -Modified thermal shutdown hysteresis value Operation : P32 -Update PGOOD threshold value I2C Register Map: P33,P36 -Update register description of [0x05] Footprint Information P39 -Add footprint information
1.1	2018-05-16	Ordering Information : P9 -Modified product P/N Top Marking Definition : P10 -Modified product P/N Typical Application Circuit : P12 -Modified circuit Electrical Characteristics : P16 -Modified product P/N Application Information : P24 -Modified product P/N Register Table and Descriptions : P33, P34, P35, P37 -Modified product P/N
1.2	2019-05-24	Order Information : P9 -Add product P/N Top Marking Definition : P10 -Add product P/N Electrical Characteristics:P13, P15, P16 -Modified absolute maximum ratings -Modified description -Add product P/N I2C interface:P25 -Modified description Functional Description:P30 -Modified functional block diagram in general description Register Table and Descriptions: P33, P34, P35 -Add product P/N -Modified register table

1.3	2019-08-20	Order Information:P10 -Add product P/N Top Marking Definition:P11 -Add product P/N Pin Assignments and Descriptions:P12 -Modified description Typical Application Circuit:P13 -Modified recommended external component P/N Electrical Characteristics: P17 -Add product P/N Typical Operating Characteristics: P18 to P23 - Add curves I2C interface:P28 -Modified description Register Table and Descriptions: P36, P38 -Add product P/N -Modified register table
1.4	2020-05-25	Order Information:P10 -Add product P/N Top Marking Definition:P11 -Add product P/N Electrical Characteristics: P17 -Add product P/N Register Table and Descriptions: P36, P38 -Add product P/N -Modified register table
1.5	2021-09-01	Overview : P7 -Updated feature description Applications : P8 -Modify Applications Top Marking Definition : P10 -Updated marking code Order Information:P10 -Add product P/N Top Marking Definition:P11 -Add product P/N Electrical Characteristics: P16, P17 -Add product P/N Application Information : P26, P27, P28, -Add LPM and I2C time out description -Modified product P/N Register Table and Descriptions: P36, P37, P38 P39, P40, P41, P42, P43, P44 -Add product P/N -Modified register table

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1 Overview

1.1 Features

- Programmable Output Voltage Range
  - 0.27V to 1.4V, 6.25mV/bit (DIE_ID Register 0x03 bit0=1)
  - 0.3V to 1.3V, 5mV/bit (DIE_ID Register 0x03 bit0=0)
- Programmable Slew Rate for Voltage Transitions
- 2.5V to 5.5V Input Voltage Range
- Steady 2.4MHz Switching Frequency
- Best-In-Class Load Transient
- Continuous Output Current Capability : 3A
- I^2C-Compatible Interface Up to 3.4Mbps
- PFM Mode for High Efficiency in Light Load
- Quiescent Current in auto PFM/PWM mode
  - 45µA in normal mode
  - 36µA in low power mode (only DIE_ID Register 0x03 bit0=1)
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 15-Ball WL-CSP Package

1.2 Applications

- Application, Graphic, and DSP Processors
  - ARM™, Tegra™, OMAP™, NovaThor™, ARMADA™, Krait™, etc.
- Hard Disk Drives, LPDDR3, LPDDR4, LPDDR4x, LPDDR5
- Tablets, Netbooks, Ultra-Mobile PCs, Personal Information Appliances
- Smart Phones
- Gaming Devices
- Industrial HMI, desktop POS, KIOSK, digital signage

1.3 General Descriptions

The MT6691 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I2C interface capable of operating up to 3.4MHz.

Using a proprietary architecture with synchronous rectification, the MT6691 is capable of delivering 3A continuously at over 80% efficiency, maintaining that efficiency at load currents as low as 10mA. The regulator operates at a nominal fixed frequency of 2.4MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, the Pulse Frequency Modulation (PFM) is used to operate in Power-Save Mode with a typical quiescent current of 45µA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 2.4MHz. In the Shutdown Mode, the supply current is typically 0.1µA, excellent in reducing power consumption. The PFM Mode can be disabled if fixed frequency is desired. The MT6691 is available in a small WL-CSP-15B 1.31x2.02 (BSC).

1.4 Ordering Information

Table 1-1. MT6691 ordering information

Product	Power-Up Defaults		EN Delay time	Package Type
	VSEL0	VSEL1		
MT6691ZVP/A	0.5V	0.6V	0ms	WL-CSP-15B 1.31x2.02 (BSC)
MT6691ZXP/A	0.4V	0.6V	3ms	
MT6691OOP/A	1.125V	1.125V	2ms	
MT6691OTP/A	1.225V	1.225V	0ms	
MT6691SVP/A	0.75V	0.75V	0ms	
MT6691ZNP/A	0.9V	0.9V	0ms	
MT6691SFP/A	0.75V	0.75V	2ms	

Table 1-2. MT6691 DIE_ID overview of feature and spec difference

DIE_ID Register 0x03	VID Range(V)	VID Resolution (mV/step)	Support Low Power Mode	Support I2C Time Out
Bit0=0	0.3 to 1.3	5	No	No
Bit0=1	0.27 to 1.4	6.25	Yes	Yes

1.5 Top Marking Definition

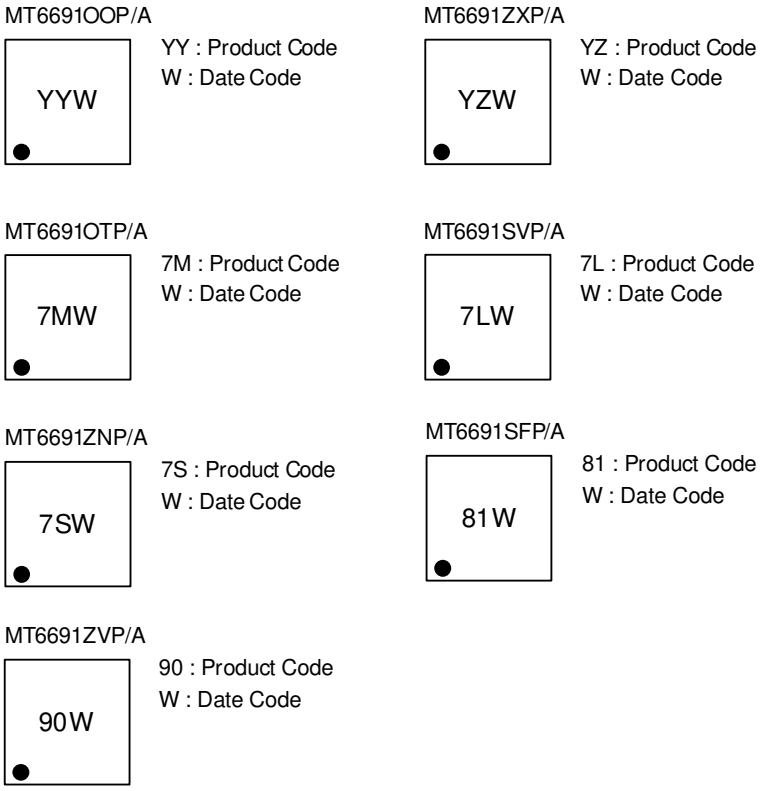


Figure 1-1. Marking information

1.6 Pin Assignments and Descriptions

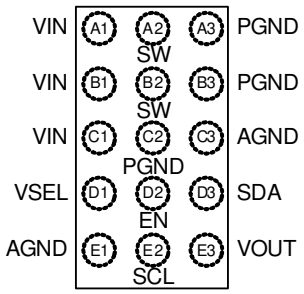


Figure 1-2. MT6691 WL-CSP-15B 1.31x 2.02 (BSC) (top view)

Table 1-3. MT6691 pin descriptions

Pin No.	Pin Name	Pin Function
A1, B1, C1	VIN	Power input voltage. Connect to the input power source. Connect to C_{IN} with minimal path.
A2, B2	SW	Switching node. Connect to the inductor.
A3, B3, C2	PGND	Power ground. The low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
C3, E1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
D1	VSEL	Voltage select. When this pin is low, V_{OUT} is set by the VSEL0 register. When this pin is high, V_{OUT} is set by the VSEL1 register. Note that the polarity of VSEL pin and the operation mode bits are conjunction with the NESL0 register, NSEL1 register and Control register 02h. Please refer to the "Register Table and Descriptions" chapter for detail output voltage and operation mode settings.
D2	EN	Enable. The device is in the Shutdown Mode when this pin is low. Device will reset all register to default when EN pin is low.
D3	SDA	I^2C serial data.
E2	SCL	I^2C serial clock.
E3	VOUT	VOUT. Output voltage sense through this pin. Connect to output capacitor.

1.7 Typical Application Circuit

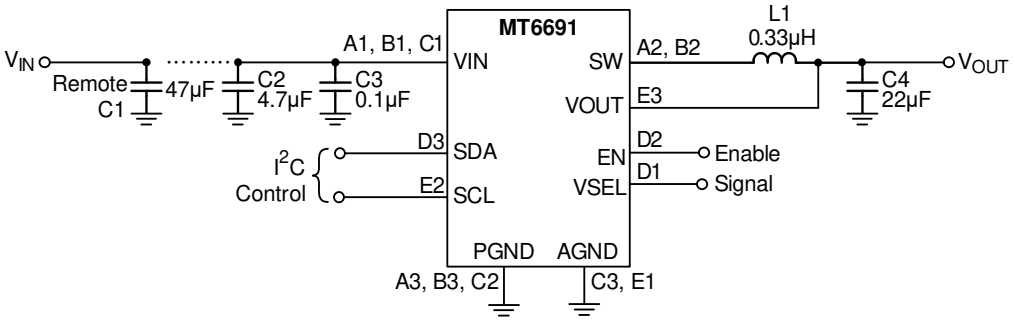


Figure 1-3. MT6691 typical application circuit

Table 1-4. Recommended external components for 3A maximum load current

Component	Description	Vendor P/N
L1	330nH, 2016 case size	DFE201610E-R33M=P2 (Murata)
		HMMQ20161T-33MDR (Cyntec)
C2	4.7µF, 10V, X5R, 0402	GRM155R61A475MEAA (Murata)
C3 (1)	100nF, 6.3V, X5R, 0201	GRM033R60J104KE19D (Murata)
C4	22µF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (Murata)
		C1608X5R0J226M080AC (TDK)

(1) Note 1 The decouple capacitor C3 is recommended to reduce any high frequency component on VIN bus.
C3 is optional and used to filter any high frequency component on VIN bus.

(2) Note 2 All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

(1)

- Supply Input Voltage, VIN ---------- -0.3V to 7V
- SW Pin Switch Voltage ---------- -1V to 7.3V
  <50ns ---------- -5V to 8.5V
- Other I/O Pin Voltages ---------- -0.3V to 7.3V
- Power Dissipation, PD @ T_A = 25°C
  WL-CSP 15B 1.31x2.02 (BSC) ---------- 2.38 W
- Package Thermal Resistance (2)
  WL-CSP-15B 1.31x2.02 (BSC), θ_{JA} ---------- 42°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- -65°C to 150°C
- ESD Susceptibility (3)
  HBM (Human Body Model) ---------- 2kV

(1) Note 1 Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

(2) Note 2 θJA is measured under natural convection (still air) at TA = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

(3) Note 3 Devices are ESD sensitive. Handling precaution recommended.

2.2 Recommended Operating Range

- Supply Input Voltage, VIN ---------- 2.5V to 5.5V
- Output Current, I_{OUT} ---------- 0A to 3A
- Junction Temperature Range ---------- -40°C to 125°C
- Ambient Temperature Range ---------- -40°C to 85°C

Note. The device is not guaranteed to function outside its operating conditions.

2.3 Electrical Characteristics

V_{IN} = 3.6V, T_A = –40°C to 85°C, unless otherwise specified

Table 2-1. Electrical specifications

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Quiescent Current PWM		I_{Q_PWM}	I_{LOAD} = 0, mode Bit = 1 (Forced PWM) (1)	--	15	--	mA
Operating Quiescent Current PFM		I_{Q_PFM}	I_{LOAD} = 0A	--	45	--	µA
Operating Low Power Mode Quiescent Current PFM		$I_{Q\_PFM\_LPM}$	I_{LOAD} = 0A and Enable LPM (2)	--	36	--	µA
H/W Shutdown Supply Current		$I_{SHDN\_H/W}$	EN = GND	--	0.1	3	µA
S/W Shutdown Supply Current		$I_{SHDN\_S/W}$	EN = V_{IN}, BUCK_ENx = 0, 2.5V ≤ V_{IN} ≤ 5.5V	--	2	12	µA
Under-Voltage Lockout Threshold		V_{UVLO}	VIN rising	--	2.32	2.45	V
Under-Voltage Lockout Hysteresis		ΔV_{UVLO}		--	350	--	mV
$R_{DS(ON)}$ of P-MOSFET		$R_{DS(ON)\_P}$	V_{IN} = 5V	--	30	--	mΩ
$R_{DS(ON)}$ of N-MOSFET		$R_{DS(ON)\_L}$	V_{IN} = 5V	--	17	--	mΩ
Input Voltage	Logic-High	V_{IH}	2.5V ≤ V_{IN} ≤ 5.5V	1.1	--	--	V
	Logic-Low	V_{IL}	2.5V ≤ V_{IN} ≤ 5.5V	--	--	0.4	
EN Input Bias Current		I_{EN}	EN input tied to GND or V_{IN}	--	0.01	1	µA
V_{OUT} DC Accuracy			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} > 0.6V, Auto PFM/PWM (1)	–3	--	3	%
			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} ≤ 0.6V, Auto PFM/PWM (1)	–18	--	18	mV
			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} > 0.6V, Force PWM (1)	–2	--	2	%
			2.8V ≤ V_{IN} ≤ 4.8V, V_{OUT} from Minimum to Maximum, $I_{OUT(DC)}$ = 0 to 3A, V_{OUT} ≤ 0.6V, Force PWM (1)	–12	--	12	mV
Load Regulation		ΔV_{LOAD}	$I_{OUT(DC)}$ = 1 to 3A (1)	--	0.1	--	%/A
Line Regulation		ΔV_{LINE}	2.5V ≤ V_{IN} ≤ 5.5V, $I_{OUT(DC)}$ = 1.5A (1)	--	0.2	--	%/V
Transient Load Response		AC_{LOAD}	I_{LOAD} step 0.01A to 1.5A, t_R = t_F = 500ns, V_{OUT} = 1.125V (1)	--	±45	--	mV
Transient Load Response		AC_{LOAD}	I_{LOAD} step 0.1A to 1.8A, t_R = t_F = 1µs, V_{IN} = 3.8V, V_{OUT} = 0.9V (1)	--	±56	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transient Load Response	AC_{LOAD}	I_{LOAD} step 0.01A to 0.8A, $t_R = t_F$ = 1µs, L = 0.33µH, C_{OUT} = 22µF x 2 (1)	--	45	--	mV
Line Transient	V_{LINE}	V_{IN} = 3V to 3.6V, $t_R = t_F$ = 10µs, I_{OUT} = 100mA, Forced PWM mode (1)	--	±40	--	mV
P-MOSFET Peak Current Limit	I_{LIM_P}		5	5.5	6	A
Valley Current Limit			3.5	4	4.5	A
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	°C
Input OVP Shutdown	V_{SDHD_OVPrth}	Rising threshold	--	6.15	--	V
Input OVP Shutdown	V_{SDHD_OVPfth}	Falling threshold	5.5	5.73	--	V
Switching Frequency	f_{SW}	V_{OUT} = default MT6691ZVP/A : 0.6V MT6691ZXP/A : 0.6V MT6691OOP/A : 1.125V MT6691SVP/A : 0.75V MT6691OTP/A : 1.225V MT6691ZNP : 0.9V MT6691SFP : 0.75V	2100	2400	2700	kHz
Minimum Off-Time	t_{OFF_MIN}		--	170	--	ns
DAC Resolution		(1)	--	8	--	bits
DAC Differential Nonlinearity		(1)	--	--	0.5	LSB

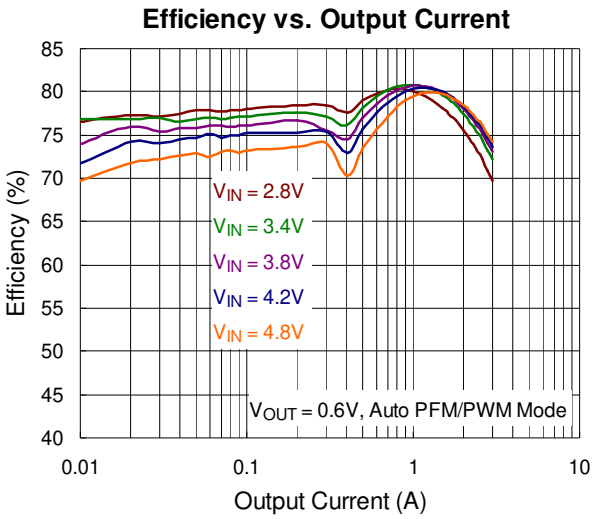
(1) Note 1 Guaranteed by design.

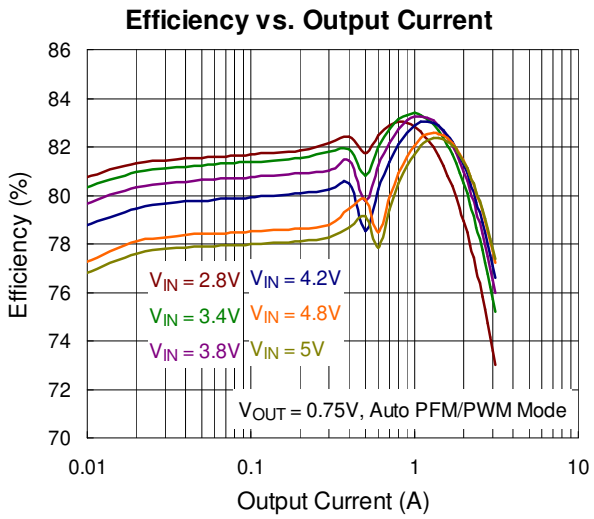
(2) Note 2 Low power mode is available only for DIE_ID Register 0x03 bit0=1.

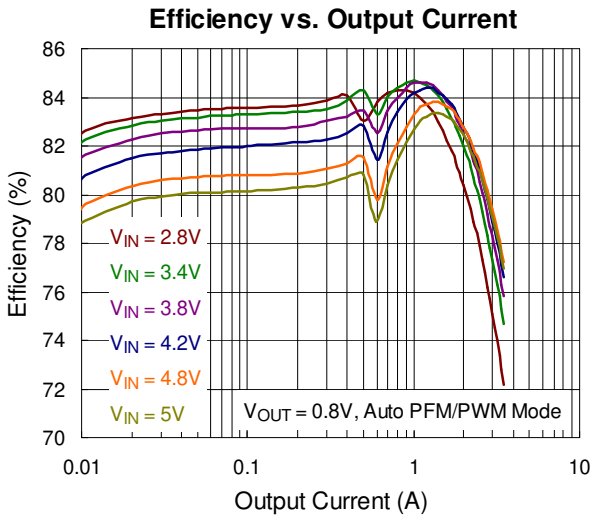
3 Typical Operating Characteristics

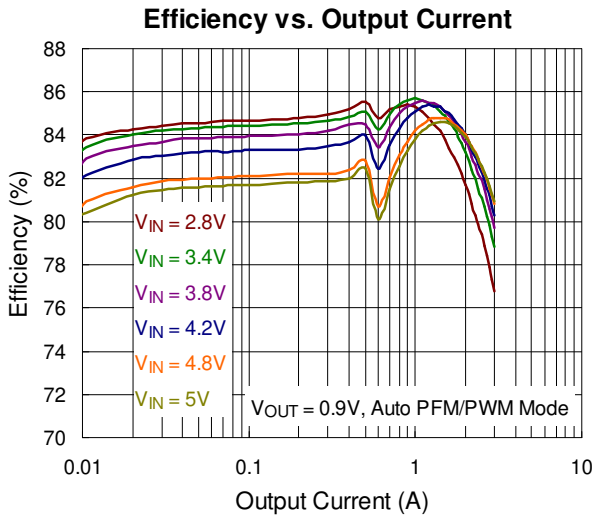
3.1 Typical Operating Characteristics

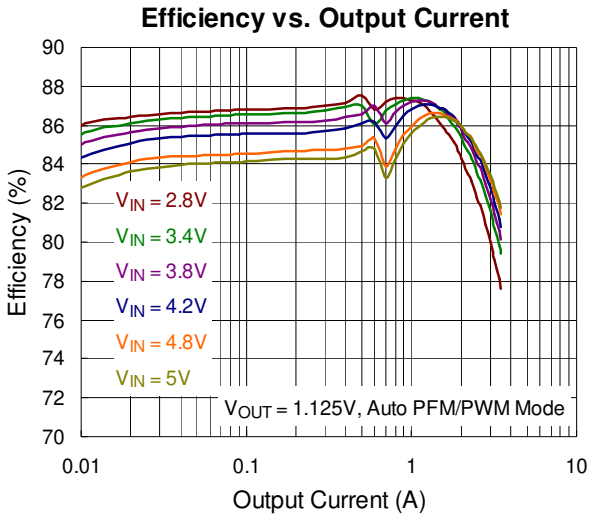
Unless otherwise specified, Auto PFM/PWM mode, V_{IN} = 3.6V, V_{EN} = V_{IN}, T_A = 25°C; circuit and components according to typical application circuit and Table 1-4.

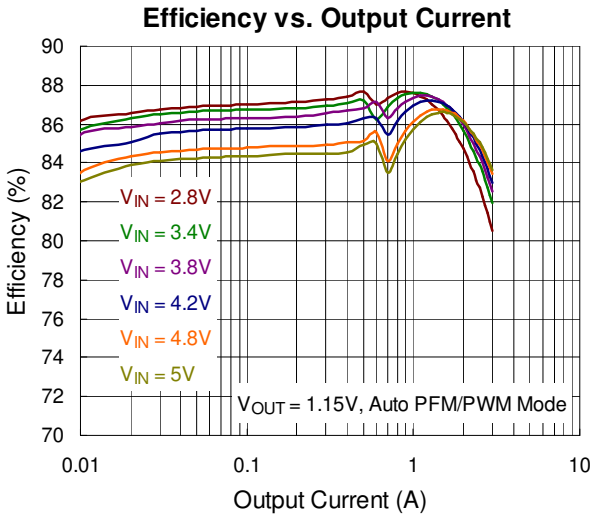


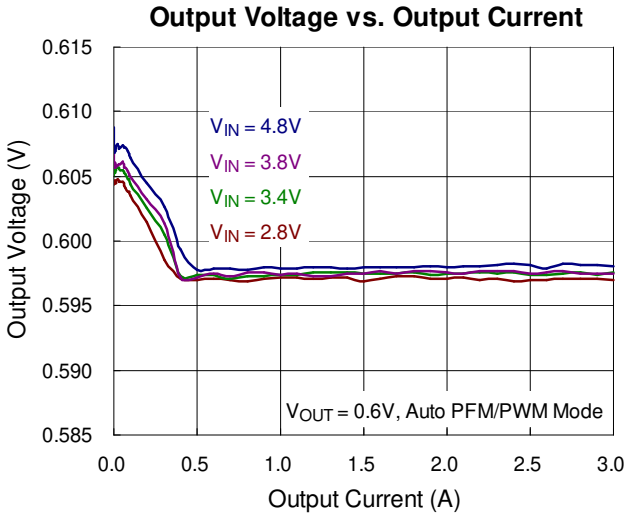


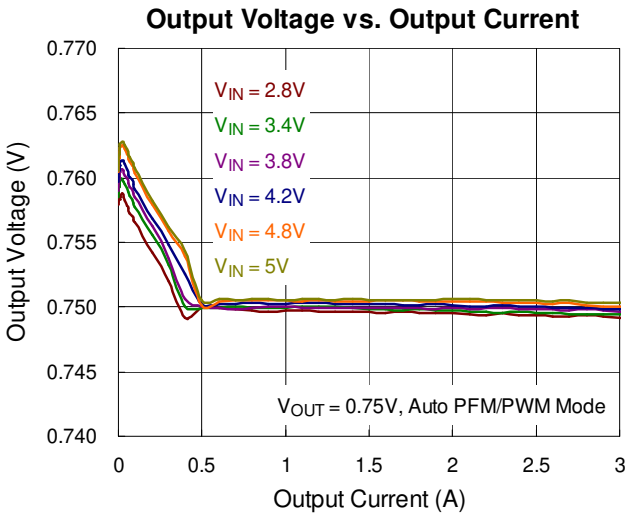


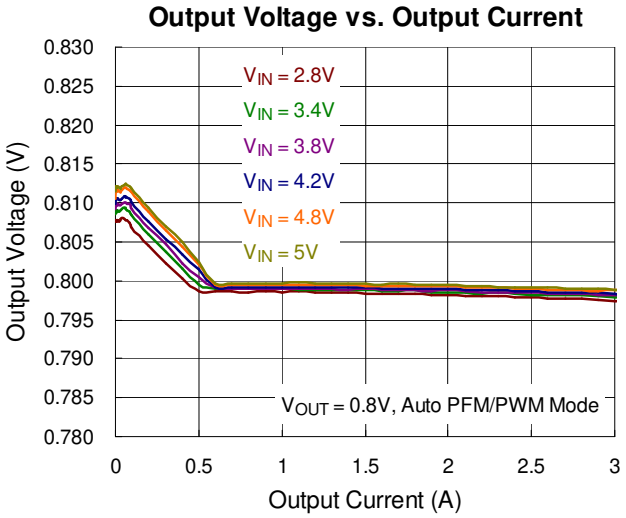


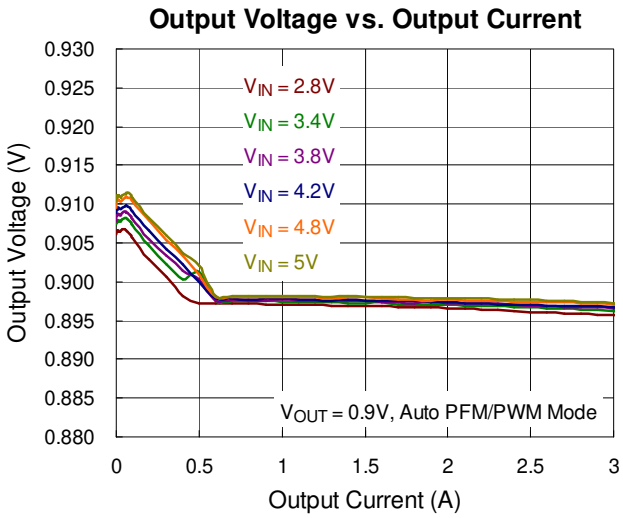




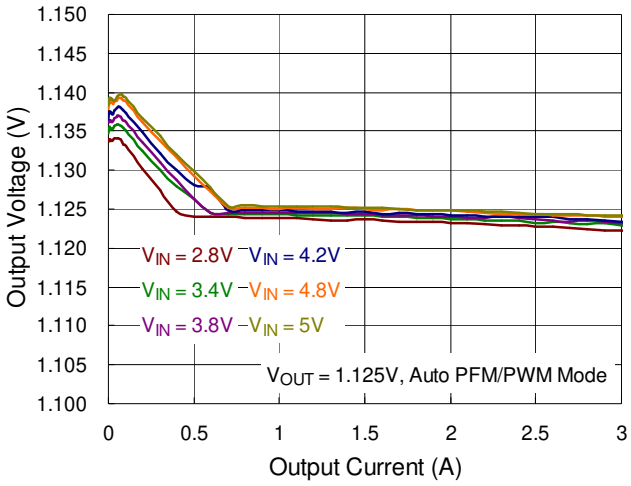




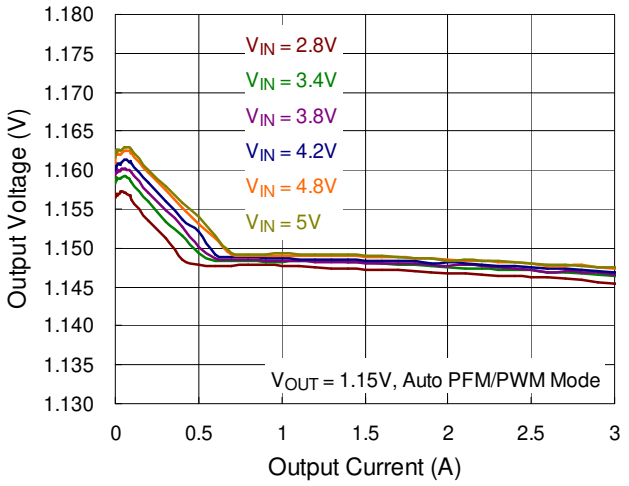




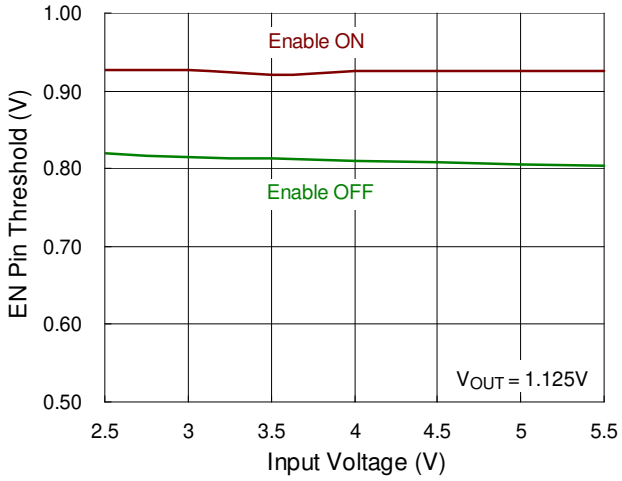
Output Voltage vs. Output Current



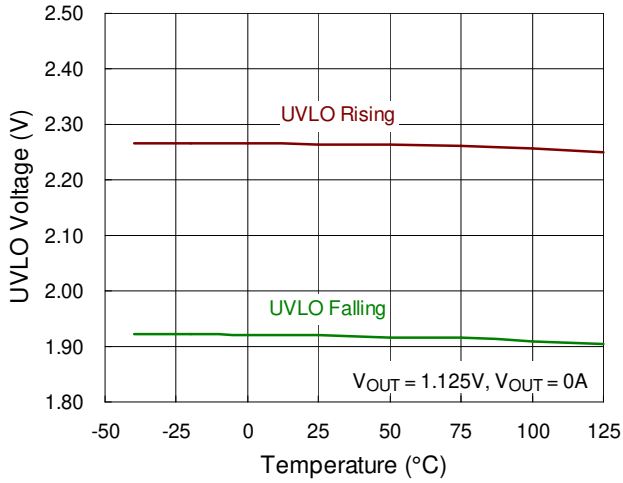
Output Voltage vs. Output Current



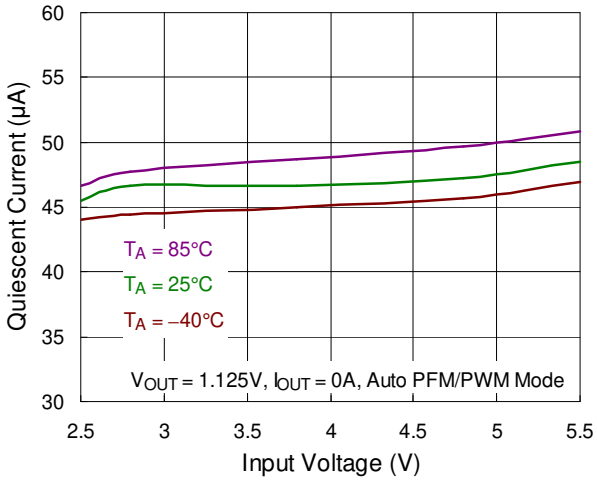
EN Pin Threshold vs. Input Voltage



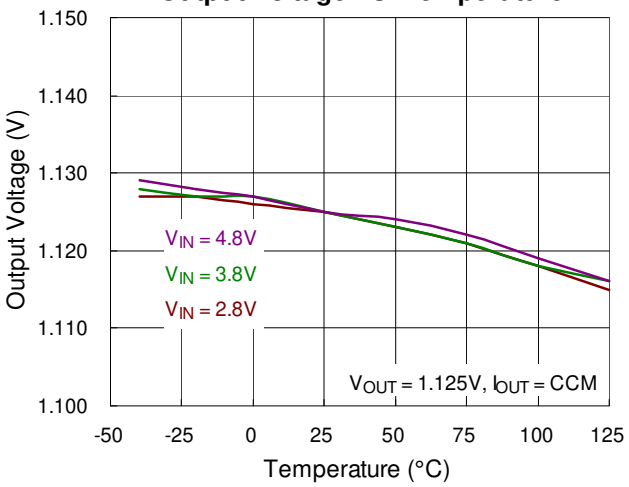
UVLO Voltage vs. Temperature



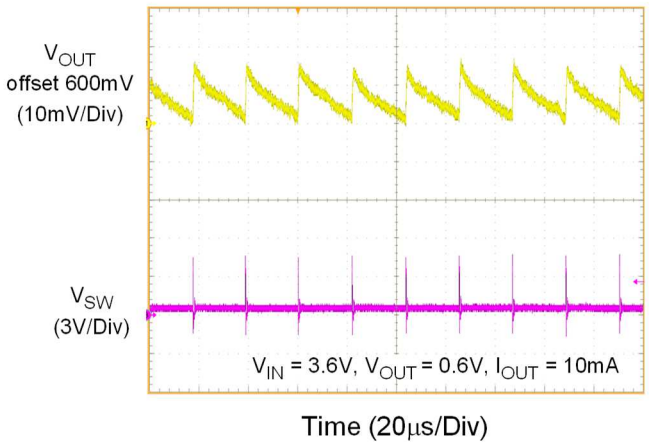
Quiescent Current vs. Input Voltage



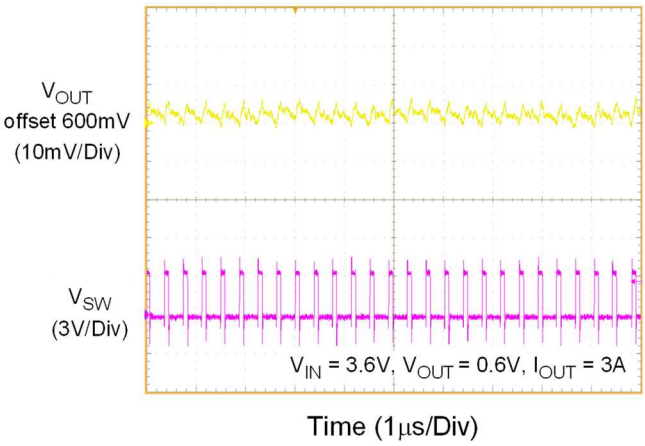
Output Voltage vs. Temperature



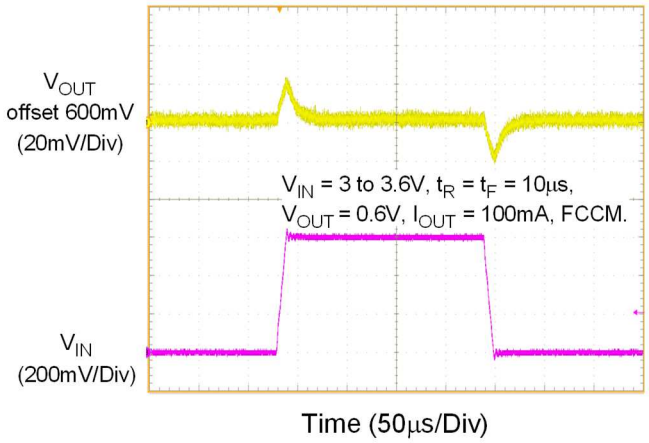
Output Ripple Voltage



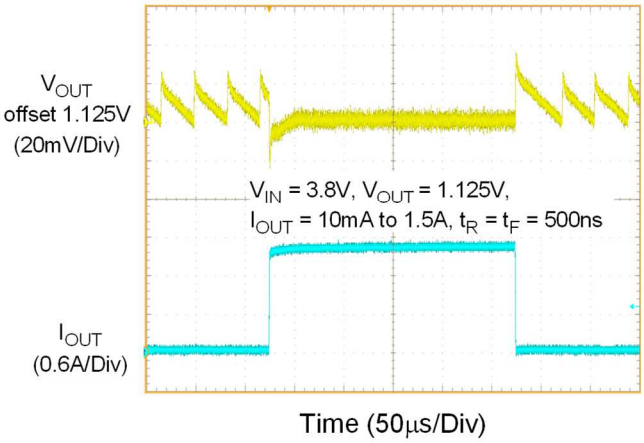
Output Ripple Voltage



Line Transient Response



Load Transient Response



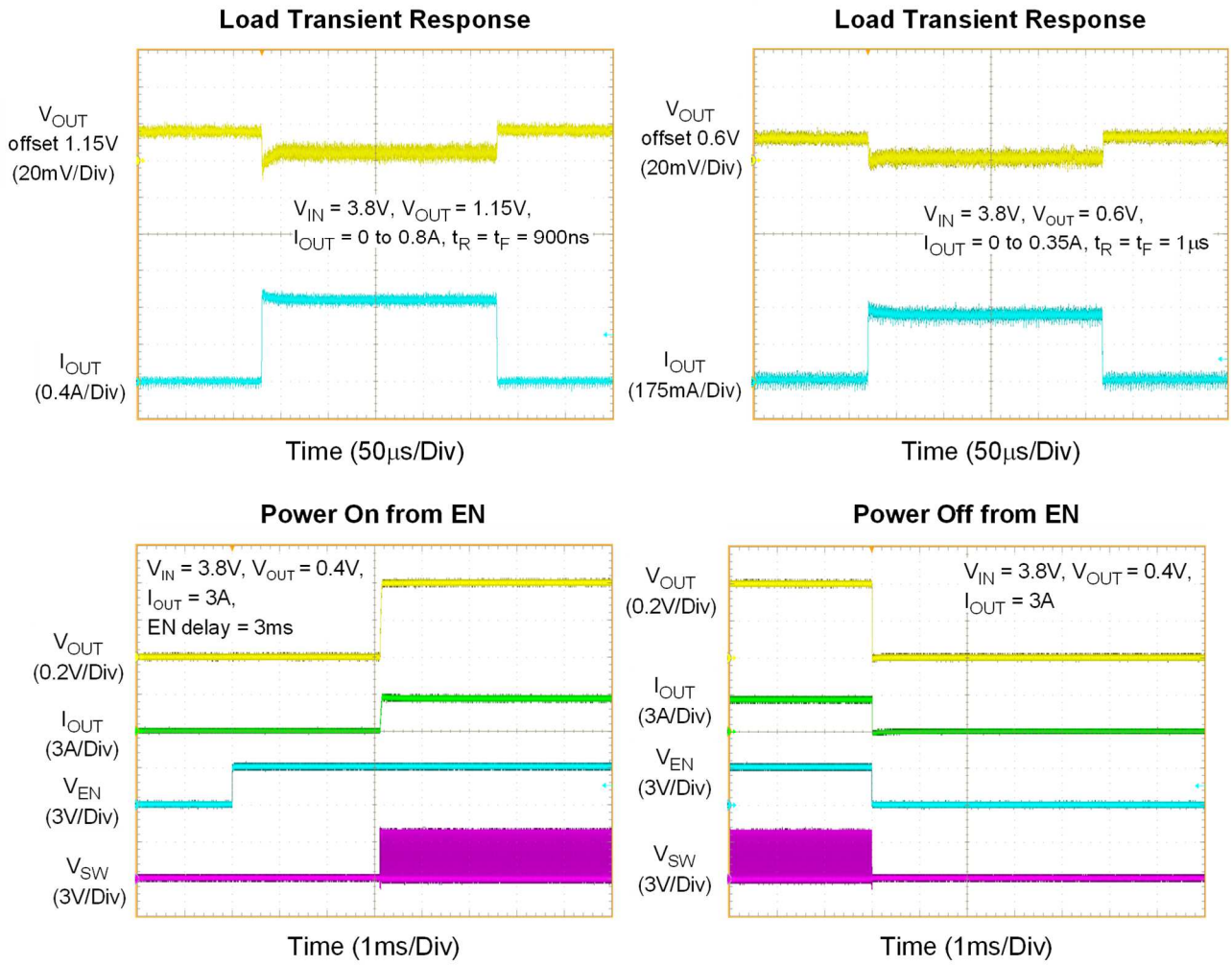


Figure 3-1. Typical operating characteristics

4 Application Information

4.1 General Descriptions

The basic MT6691 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

4.2 Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance, as shown in equation below :

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. Thus, a large inductor is required to attain this goal.
The largest ripple current occurs at the highest V_{IN}. A reasonable starting point for selecting the ripple current is ΔI_L = 0.3 x I_{MAX} to 0.4 x I_{MAX}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

4.3 Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET.

To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)} / 2$.
This simple worst-case condition is commonly used for design.

Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications.

However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output voltage ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

Where fSW is the switching frequency and ΔI_L is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement.
Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Nevertheless, high value, low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications.

4.4 I²C Interface Function

The MT6691 can be used by I²C interface to select V_{OUT} voltage level; Dynamic Voltage Scaling (DVS) slew rate, Auto PFM/PSM or FCCM mode, and so on.

The register of each function can be found from the following register map and it also explains how to use these function.

4.5 V_{OUT} Selection

The MT6691 all series products have two kinds of programmable output voltage range and can be recognized by DIE_ID Register (0x03 bit0). For DIE_ID Register 0x03 bit0=1, V_{OUT} can be adjusted from 0.27V to 1.4V with 6.25mV/bit resolution. On the other hand, for DIE_ID Register 0x03 bit0=0, V_{OUT} can be adjusted from 0.3V to 1.3V with 5mV/bit resolution. Note that, the output voltage can be set by NSELx register bit and the output voltage are given by the following equation and examples :

For DIE_ID Register 0x03 bit0=1:

VOUT = 0.27V + NSELx x 6.25mV
For example:

if NSELx = 0111100 (60 decimal), then
VOUT = 0.27 + 60 x 6.25mV
= 0.27 + 0.375 = 0.645V.

For DIE_ID Register 0x03 bit0=0:

VOUT = 0.3V + NSELx x 5mV
For example:

if NSELx = 0111100 (60 decimal), then
VOUT = 0.3 + 60 x 5mV
= 0.3 + 0.3 = 0.6V.

The MT6691 also has external VSEL pin to select NSEL1(0x01) or NSEL0(0x00). Pull VSEL to high is for VSEL1 and pull VSEL to low is for VSEL0.

Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

4.6 Enable and Soft-Start

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I^2C cannot be written or read until input voltage is above the UVLO. The registers will reset when the EN pin is LOW or during a Power On Reset (POR).

Upon EN pin is high, V_{OUT} will ramp up at the chosen soft-start slew rate which is programmed in the CONTROL2 register SS_SR bit.

Raising EN while the EN_VSELx bit is HIGH activates the part and begins the soft-start cycle. For the MT6691ZXP/A and MT6691OOP/A, there are 3ms and 2ms delay time from EN HIGH to V_{OUT} start soft-start separately. And for options the MT6691SVP/A and MT6691OTP/A, there is no EN Delay and default disable EN_VSELx, V_{OUT} will begin soft-start cycle as long as EN_VSELx is enable and EN pin is set to logic high.

4.7 Discharge Function

In the CONTROL1 register, set DISCHG bit to 1 can let V_{OUT} discharge by internal resistor when converter shuts down. If set the DISCHG bit to 0, V_{OUT} will decrease depending on the loading. When EN pin is set to low, the MT6691 will default turn on internal 11Ω discharge resistor.

4.8 Slew Rate Setting

The MT6691 can control slew rate as V_{OUT} changing between two voltage levels for both up and down.
In the CONTROL1 register, DVS_UP bits can control up-speed. In the CONTROL2 register, DVS_DN can control down-speed. The default slew rate of DVS_UP is 12mV/µs and the slew rate of DVS_DN is 3mV/µs for DIE_ID Register 0x03 bit0=0. The details of slew rate setting can be found in the register function description table.

4.9 Force PWM Mode

In the CONTROL1 register, MODE_VSEL0 and MODE_VSEL1 can decide whether the converter is always at FCCM mode or enters power saving mode at light load conditions.
The default operation mode of MODE_VSEL0 is auto PFM mode and MODE_VSEL1 can be selected by factory setting.

During output voltage is changing from high to low, the MT6691 will make transition operation at PWM mode and output voltage will decrease quickly.

4.10 Low Power Mode(LPM)

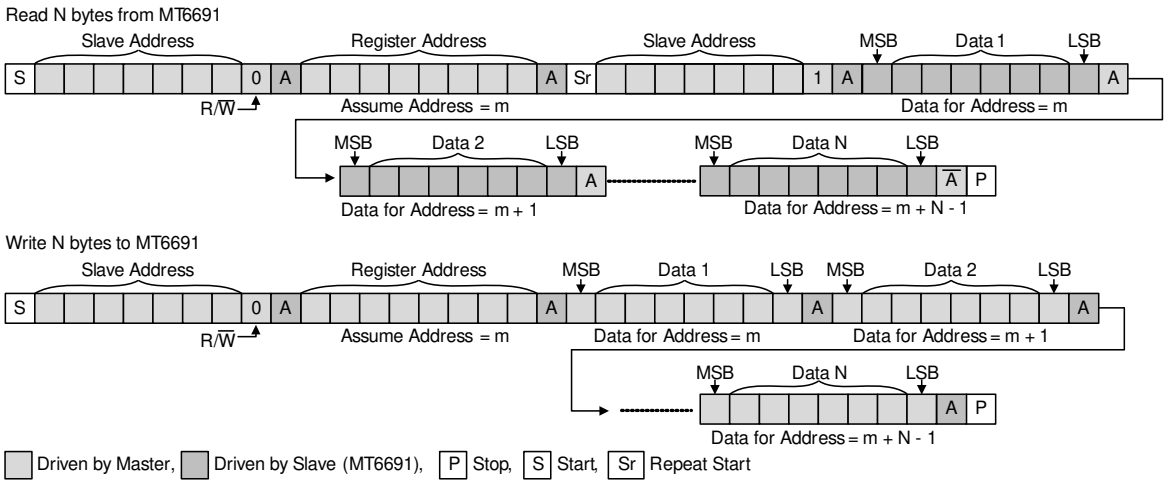
MT6691 features auto PFM/PWM mode operation to achieve power save that generates a single switching pulse to ramp up the inductor current and recharges the output capacitor, followed by a skip pulse or a sleep period to cut down current demand from input source to obtain high efficient at light load conditions. During this time, the load current is supported by the output capacitor and the duration of the sleep period depends on the load current and the inductor peak current. When system request further quiescent current reduction situation, such as shipping mode or suspend operation etc. to minimize the battery energy consumption.
The MT6691 also features the low power mode (LPM) operation, where several of the internal protection circuits (input OVP, UVP) are shut down to achieve lowest 36μA operating quiescent current for ultra-light load condition. This LPM operation can be enabled by setting LPM control register (0x0A bit1) to 1 in the CONTROL5 register, to activate the low power mode.
Note that, this LPM feature only supports with DIE_ID Register 0x03 bit0=1.

4.11 I^2C Time Out Function

The I^2C time out function is built-in to have MT6691 resume listening state during communication bus error situation. When MT6691 detects that the SCL pin is pulled down for more than 30ms or the SDA pin is pulled down by the MT6691 for more than 30ms, MT6691 will reset its I_2C interface. The SCL timeout function can be enabled or disabled by control register (0x0A bit0), for more detail setting value please refer to I_2C register table.

4.12 I^2C Interface

The all series of MT6691 are able to support fast mode I^2C interface (bit rate 400kb/s), and different parts have its own slave address. For example, the default I^2C slave address of the MT6691ZXP is 7'b1010000. The write or read bit stream (N ≥ 1) is shown below :



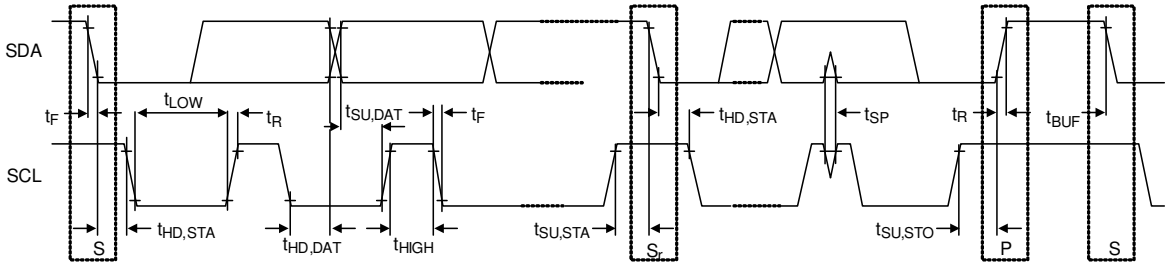


Figure 4-1. I²C read and write stream and timing diagram

The MT6691 also supports High-speed mode (bit rate up to 3.4Mb/s) with access code 08H. Figure 4-2 and Figure 4-3 show detail transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode) :

- START condition (S)
- 8-bit master code (00001xxx)
- not-acknowledge bit (Ā)

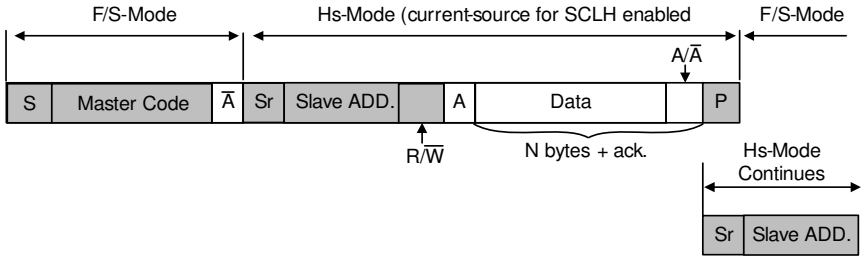


Figure 4-2. Data transfer format in HS-mode

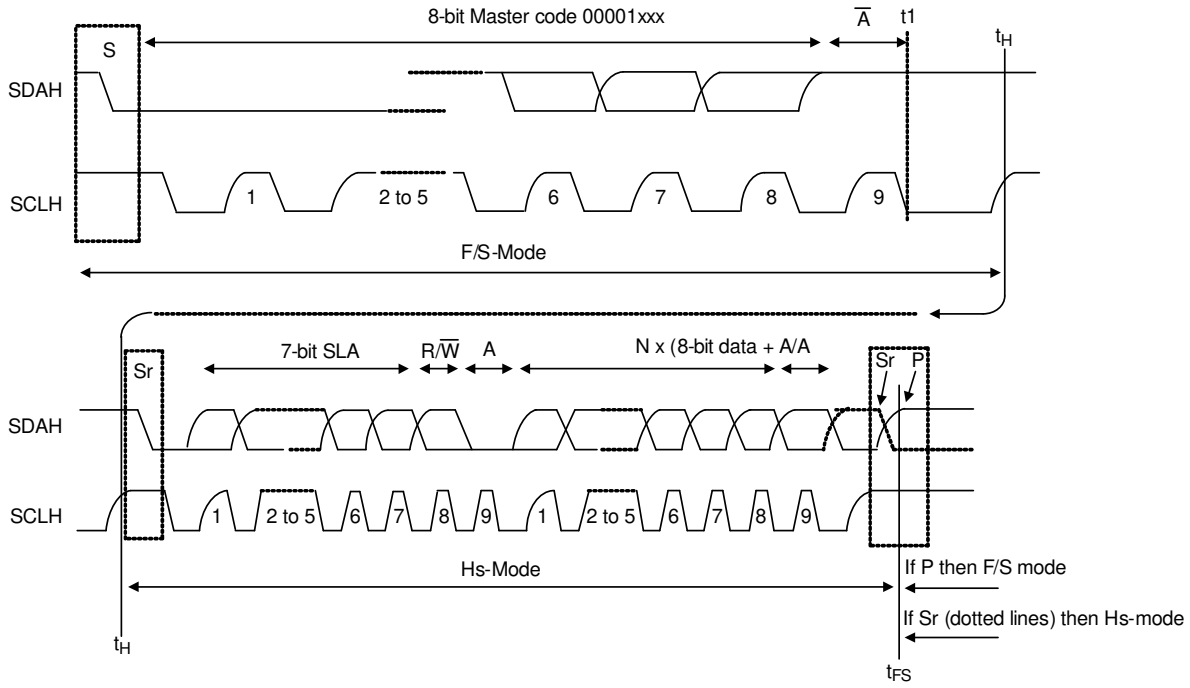


Figure 4-3. A complete HS-mode transfer

4.13 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-15B 1.31x2.02 (BSC) package, the thermal resistance, θ_{JA}, is 42°C /W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (42°C /W) = 2.38W for a WL-CSP-15B 1.31x2.02 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 4-4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

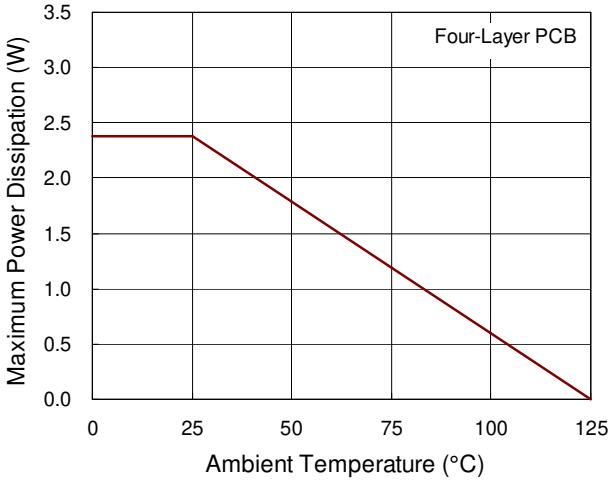


Figure 4-4. Derating curve of maximum power dissipation

4.14 Layout Considerations

For best performance of the MT6691, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to IC to minimize the power loop area. A typical 0.1µF decouple capacitor is recommended to reduce power loop area and any high frequency component on VIN.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- The AGND pin is suggested to connect to 2nd GND plate through top to 2nd via.

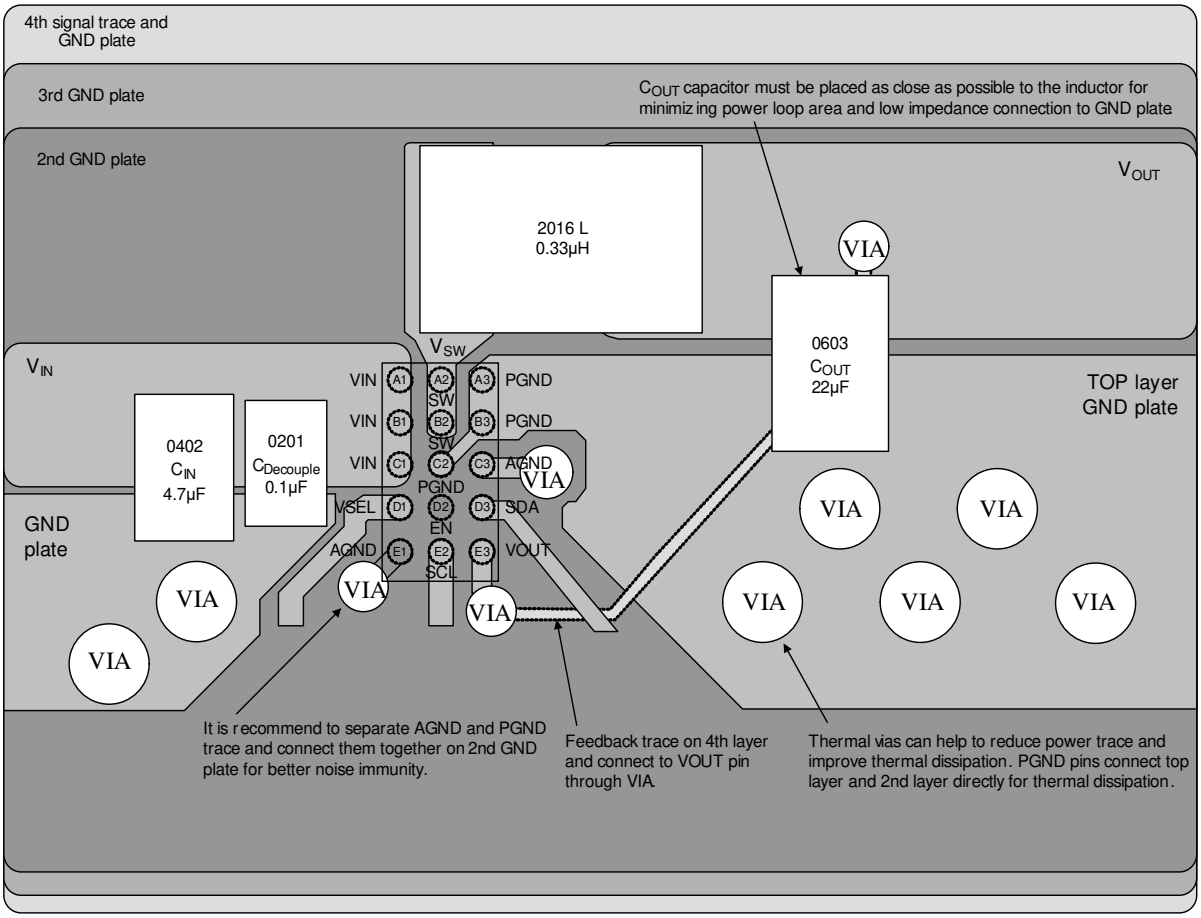
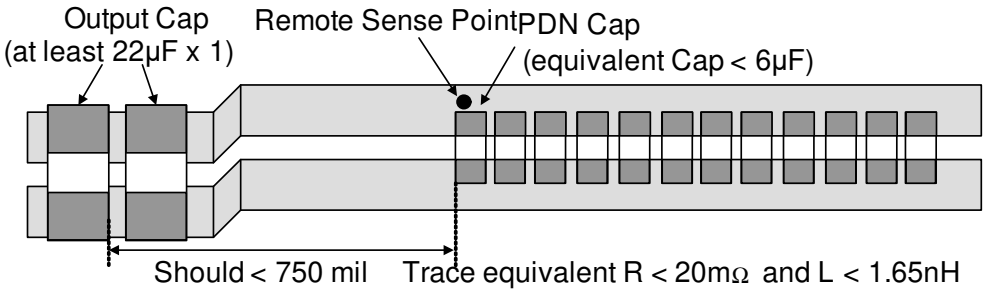
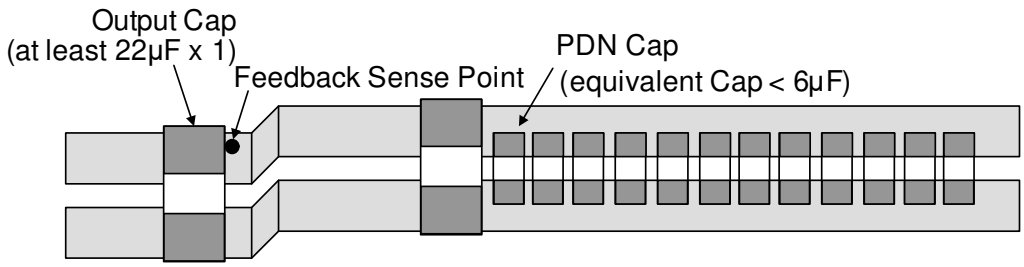


Figure 4-5. PCB layout guide

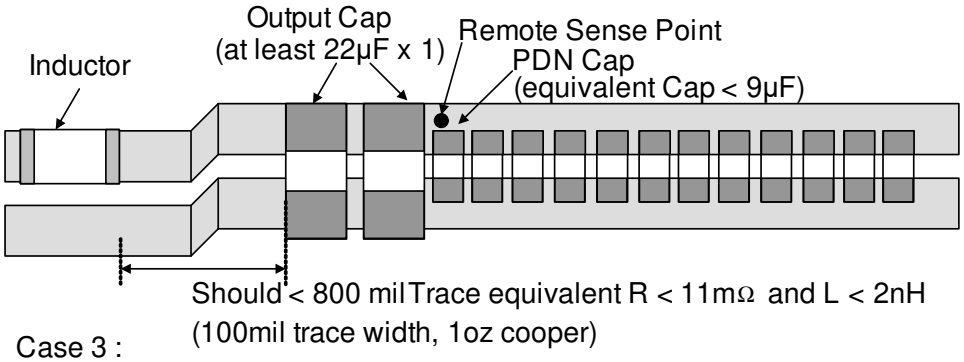
4.15 Layout Constrains for Remote Sense Applications



Case 1 :
If the remote sense point is locate d at PDN cap
, the distance between 1st 22µF cap and PDN cap should be less than 750 mil.



Case 2 :
If the remote sense point is locate d at 1st 22µF cap
, there will be no constrain between 1st 22µF cap and PDN cap yet sacrifice AP transient performance with this configuration .



Case 3 :
If the remote sense point is locate d at PDN cap and there's long trace between 1st 22µF cap and inductor, the distance should be less than 800mil.

Figure 4-6. Layout constrains

5 Functional Descriptions

5.1 General Descriptions

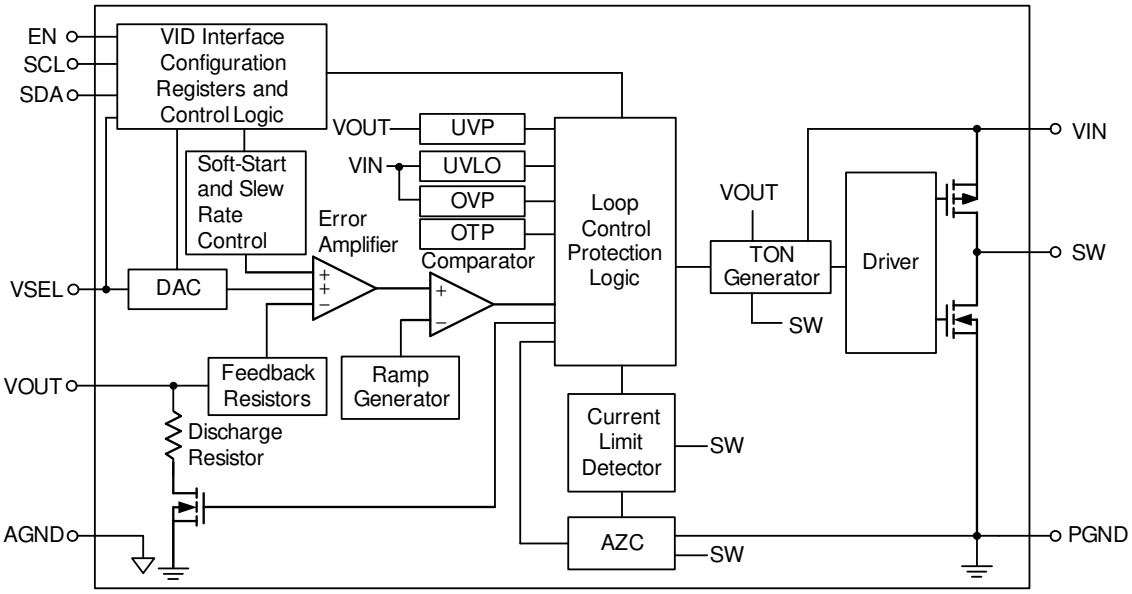


Figure 5-1. MT6691 functional block diagram

6 Operation

6.1 General Descriptions

The MT6691 is a low voltage synchronous step-down converter that supports input voltage ranging from 2.5V to 5.5V and the output current can be up to 3A. The MT6691 uses ACOT® mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allows the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

6.2 PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation :

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

Where fSW is nominal 2.4MHz

6.3 Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decrease to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can adjust for different conditions to get better efficiency.

6.4 Under-Voltage Protection (UVLO)

The UVLO continuously monitors the voltage of VIN to make sure the device works properly. When the VCC is high enough to reach the high threshold voltage of UVLO. The step-down converter softly starts or pre-biases to its regulated output voltage. When the VIN decreases to its low threshold (350mV hysteresis), the device will shut down.

6.5 Power GOOD

When the output voltage is higher than PGOOD rising threshold (86% of its setting voltage), the PGOOD flag is high.

6.6 Output Under-Voltage Protection (UVP) and Over-Current Protection (OCP)

When the output voltage of the MT6691 is lower than 59% of the reference voltage after soft-start, the UVP is triggered. The MT6691 senses the current signal when high-side and low-side MOSFET turns on. As a result, the OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next pulse and turns on low-side switch until inductor drops below the valley current limit, and then turns on high-side again to maintain output voltage and supports loading current to output before triggering UVP.

If the OCP condition keeps and the load current is larger than the current which converter can provide, the output voltage will decrease and drop below UVP threshold, and converter will keep switching for 16 consecutive cycles before converter enters hiccup operation. The converter latches off 1.7ms when the output voltage is still lower than UVP threshold, and the soft-start sequence begins again after latching off time.

Note that, there is sensing propagation delay time before triggering OCP; hence, the OCP may take few cycles to occur while the inductor current near OCP threshold. If the output voltage drop slowly before entering hiccup operation, the converter will extend the high-side switch on-time and turns on low-side switch for only minimum off-time to provide large load current and catch up with the output voltage before detecting peak current limit OCP.

6.7 Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time can be programming by I^2C.

6.8 Over-Temperature Protection (OTP)

The MT6691 has over-temperature protection. When the device triggers the OTP, the device shuts down immediately, and will soft-start again while the junction temperature below recovery threshold.

7 Register Table and Descriptions

7.1 I²C Register Map

The MT6691ZXP/A I²C slave address = 7'b1010000 for 0.4V/0.6V setting.
The MT6691OOP/A I²C slave address = 7'b1010111 for 1.125V/1.125V setting.
The MT6691SVP/A I²C slave address=7'b1010001 for 0.75V/0.75V setting.
The MT6691OTP/A I²C slave address=7'b1010110 for 1.225V/1.225V setting.
The MT6691ZNP/A I²C slave address = 7'b1010101 for 0.9V/0.9V setting.
The MT6691SFP/A I²C slave address is 7'b1010010 for 0.75V/0.75V setting.

Note that, MT6691 all series products have two kinds of programmable output voltage range and can be recognized by DIE_ID Register (0x03 bit0). For DIE_ID Register 0x03 bit0=1, V_{OUT} can be adjusted from 0.27V to 1.4V with 6.25mV resolution. On the other hand, for DIE_ID Register 0x03 bit0=0, V_{OUT} can be adjusted from 0.3V to 1.3V with 5mV resolution. Hence, the I²C register map will point out two kinds of product according to DIE_ID Register, please find the corresponding settings.
The I²C register map is introduced in the following table:

Table 7-1. I2C register map

Address Name	Register Address		Part No.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NSEL0 (DIE_ID Register 0x03 bit0=0)	0x00	Meaning	VSEL0								
		Default	MT6691ZVP/A	0	0	1	0	1	0	0	0
			MT6691ZXP/A	0	0	0	1	0	1	0	0
			MT6691OOP/A	1	0	1	0	0	1	0	1
			MT6691SVP/A	0	1	0	1	1	0	1	0
			MT6691OTP/A	1	0	1	1	1	0	0	1
			MT6691ZNP/A	0	1	1	1	1	0	0	0
			MT6691SFP/A	0	1	0	1	1	0	1	0
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL0 (DIE_ID Register 0x03 bit0=1)	0x00	Meaning	VSEL0								
		Default	MT6691ZVP/A	0	0	1	0	0	1	0	1
			MT6691ZXP/A	0	0	0	1	0	1	0	1
			MT6691OOP/A	1	0	0	0	1	0	0	1
			MT6691SVP/A	0	1	0	0	1	1	0	1
			MT6691OTP/A	1	0	0	1	1	0	0	1
			MT6691ZNP/A	0	1	1	0	0	1	0	1
			MT6691SFP/A	0	1	0	0	1	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL1 (DIE_ID Register	0x01	Meaning	VSEL1								
		Default	MT6691ZVP/A	0	0	1	1	1	1	0	0
			MT6691ZXP/A	0	0	1	1	1	1	0	0
			MT6691OOP/A	1	0	1	0	0	1	0	1

0x03 bit0=0)			MT6691SVP/A	0	1	0	1	1	0	1	0
			MT6691OTP/A	1	0	1	1	1	0	0	1
			MT6691ZNP/A	0	1	1	1	1	0	0	0
			MT6691SFP/A	0	1	0	1	1	0	1	0
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL1 (DIE_ID Register 0x03 bit0=1)	0x01	Meaning	VSEL1								
		Default	MT6691ZVP/A	0	0	1	1	0	1	0	1
			MT6691ZXP/A	0	0	1	1	0	1	0	1
			MT6691OOP/A	1	0	0	0	1	0	0	1
			MT6691SVP/A	0	1	0	0	1	1	0	1
			MT6691OTP/A	1	0	0	1	1	0	0	1
			MT6691ZNP/A	0	1	1	0	0	1	0	1
			MT6691SFP/A	0	1	0	0	1	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONTROL1	0x02	Meaning	DISCHG	UP_SR[2:0]			Reserved	SW_ RESET	MODE_ VSEL1	MODE_ VSEL0
		Default	1	0	0	1	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
ID1 (DIE_ID Register 0x03 bit0=0)	0x03	Meaning	VENDOR_ID			Reserved	DIE_ID			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
ID1 (DIE_ID Register 0x03 bit0=1)	0x03	Meaning	VENDOR_ID			Reserved	DIE_ID			
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R
ID2	0x04	Meaning	Reserved				DIE_REV			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MONITOR	0x05	Meaning	PGOOD	UVLO	Reserved	POS	NEG	RESET_ STAT	OT	BUCK_ STATUS
		Default	0	0	--	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
CONTROL2	0x06	Meaning	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_ VSEL1	EN_ VSEL0
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
CONTROL4	0x08	Meaning	Reserved		DIS_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0

		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
CONTROL5 (Only for DIE_ID Register 0x03 bit0=1)	0x0A	Meaning	Reserved						LPM	REG_I2C_TIME_OUT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R/W	R/W

The I²C register function description is introduced in the following table:

Table 7-2. I2C register function description

Register Name	Register Address		Part No.	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
NSEL0 (DIE_ID Register 0x03 bit0=0)	0x00	Meaning	VSEL0								
		Default	MT6691ZVP/A	0	0	1	0	1	0	0	0
			MT6691ZXP/A	0	0	0	1	0	1	0	0
			MT6691OOP/A	1	0	1	0	0	1	0	1
			MT6691SVP/A	0	1	0	1	1	0	1	0
			MT6691OTP/A	1	0	1	1	1	0	0	1
			MT6691ZNP/A	0	1	1	1	1	0	0	0
			MT6691SFP/A	0	1	0	1	1	0	1	0
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL0 (DIE_ID Register 0x03 bit0=1)	0x00	Meaning	VSEL0								
		Default	MT6691ZVP/A	0	0	1	0	0	1	0	1
			MT6691ZXP/A	0	0	0	1	0	1	0	1
			MT6691OOP/A	1	0	0	0	1	0	0	1
			MT6691SVP/A	0	1	0	0	1	1	0	1
			MT6691OTP/A	1	0	0	1	1	0	0	1
			MT6691ZNP/A	0	1	1	0	0	1	0	1
			MT6691SFP/A	0	1	0	0	1	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VSEL0			For DIE_ID Register 0x03 bit0=0 VID table satisfy : SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 00000000 : 0.3V 5mV step for 0.3V to 1.3V				For DIE_ID Register 0x03 bit0=1 VID table satisfy : SEL[7:0] = 10110101: VOUT = 1.40125V … SEL[7:0] = 00000000 : 0.27V 6.25mV step for 0.27V to 1.40125V				

Register Name	Register Address		Part No	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
NSEL1 (DIE_ID Register 0x03 bit0=0)	0x01	Meaning	VSEL1								
		Default	MT6691ZVP/A	0	0	1	1	1	1	0	0
			MT6691ZXP/A	0	0	1	1	1	1	0	0
			MT6691OOP/A	1	0	1	0	0	1	0	1
			MT6691SVP/A	0	1	0	1	1	0	1	0
			MT6691OTP/A	1	0	1	1	1	0	0	1
			MT6691ZNP/A	0	1	1	1	1	0	0	0
			MT6691SFP/A	0	1	0	1	1	0	1	0
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL1	0x01	Meaning	VSEL1								

(DIE_ID Register 0x03 bit0=1)		Default	MT6691ZVP/A	0	0	1	1	0	1	0	1
			MT6691ZXP/A	0	0	1	1	0	1	0	1
			MT6691OOP/A	1	0	0	0	1	0	0	1
			MT6691SVP/A	0	1	0	0	1	1	0	1
			MT6691OTP/A	1	0	0	1	1	0	0	1
			MT6691ZNP/A	0	1	1	0	0	1	0	1
			MT6691SFP/A	0	1	0	0	1	1	0	1
		Read/Write	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VSEL1			For DIE_ID Register 0x03 bit0=0 VID table satisfy : SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 00000000 : 0.3V 5mV step for 0.3V to 1.3V				For DIE_ID Register 0x03 bit0=1 VID table satisfy : SEL[7:0] = 10110101: VOUT = 1.40125V … SEL[7:0] = 00000000 : 0.27V 6.25mV step for 0.27V to 1.40125V				

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL1	0x02	Meaning	DISCHG	UP_SR[2:0]			Reserved	SW_ RESET	MODE_ VSEL1	MODE_ VSEL0
		Default	1	0	0	1	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DISCHG			0 : Disable internal output discharge resistor							
			1 : Enable internal output discharge resistor							
UP_SR[2:0]			For DIE_ID Register 0x03 bit0=0 DVS speed for up DVS 000 = 24mV step/µs 001 = 12mV step/µs (default) 010 = 6mV step/µs 011 = 3mV step/µs 100 = 1.5mV step/µs 101 = 0.75mV step/µs 110 = 0.375mV step/µs 111 = 0.1875mV step/µs			For DIE_ID Register 0x03 bit0=1 DVS speed for up DVS 000 = 25mV step/µs 001 = 12.5mV step/µs(default) 010 = 6.25mV step/µs 011 = 3.1mV step/µs 100 = 1.56mV step/µs 101 = 0.75mV step/µs 110 = 0.39mV step/µs 111 = 0.19mV step/µs			
W_RESET			write 1 to reset, always read 0							
MODE_VSEL1			0 : Auto PFM/PWM mode							
			1 : Forced PWM mode							
MODE_VSEL0			0 : Auto PFM/PWM mode							
			1 : Forced PWM mode							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
ID1	0x03	Meaning	VENDOR_ID[2:0]			Reserved	DIE_ID[3:0]			
		Default	0	0	0	0	0	0	0	0/1
		Read/Write	R	R	R	R	R	R	R	R
VENDOR_ID[2:0]			Vendor_ID							
DIE_ID[3:0]			0: VOUT can be adjusted from 0.3V to 1.3V with 5mV resolution, no LPM feature.							

			1: VOUT can be adjusted from 0.27V to 1.4V with 6.25mV resolution, equipped with low power mode feature.							
Register Name	**Register Address**		**b[7] (MSB)**	**b[6]**	**b[5]**	**b[4]**	**b[3]**	**b[2]**	**b[1]**	**b[0] (LSB)**
ID2	0x04	Meaning	Reserved				DIE_REV[3:0]			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
DIE_REV[3:0]			Revision_ID							

Register Name	**Register Address**		**b[7] (MSB)**	**b[6]**	**b[5]**	**b[4]**	**b[3]**	**b[2]**	**b[1]**	**b[0] (LSB)**
MONITOR	0x05	Meaning	PGOOD	UVLO	Reserved	POS	NEG	RESET_ STAT	OT	BUCK_ STATUS
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
PGOOD			1 : Buck is enabled and soft-start is completed.							
UVLO			1 : Signifies the V_{IN} is less than the UVLO threshold.							
POS			1 : Signifies a positive voltage transition is in progress							
NEG			1 : Signifies a negative voltage transition is in progress							
RESET_STAT			1 : Indicates that a register reset was performed.							
OT			1 : Signifies the thermal shutdown is active.							
BUCK_STATUS			1 : Buck enabled; 0 : buck disabled.							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL2	0x06	Meaning	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_ VSEL1	EN_VSE L0
		Default	0	1	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
DN_SR[2:0]			For DIE_ID Register 0x03 bit0=0 DVS speed for DN DVS 000 = 24mV step/µs 001 = 12mV step/µs 010 = 6mV step/µs 011 = 3mV step/µs (default) 100 = 1.5mV step/µs 101 = 0.75mV step/µs 110 = 0.375mV step/µs 111 = 0.1875mV step/µs			For DIE_ID Register 0x03 bit0=1 DVS speed for up DVS 000 = 25mV step/µs 001 = 12.5mV step/µs 010 = 6.25mV step/µs 011 = 3.1mV step/µs(default) 100 = 1.56mV step/µs 101 = 0.75mV step/µs 110 = 0.39mV step/µs 111 = 0.19mV step/µs				
SS_SR[1:0]			DVS speed for soft-start DVS 00=10mV step/µs (default) 01=5mV step/µs 10=2.5mV step/µs 11=1.25mV step/µs							

EN_VSEL1	Software power on/off control register (activate when VSEL pin set to logic-high): 0 : Disable output 1 : Enable output
EN_VSEL0	Software power on/off control register (activate when VSEL pin set to logic-low): 0 : Disable output 1 : Enable output

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL4	0x08	Meaning	Reserved		DIS_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
DIS_DLY[5:0]			Delay applied upon disable (ms) 000000b = 0ms 111111b = 63ms (steps of 1ms)							

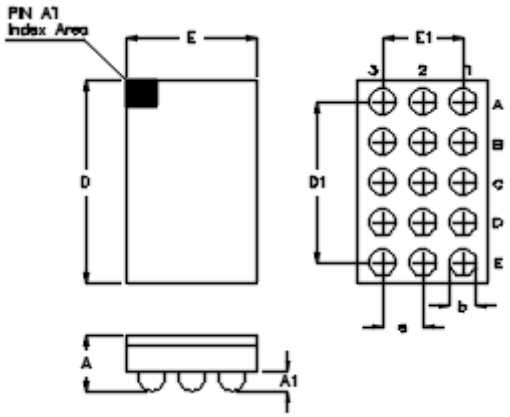
This register is only existing in DIE_ID Register 0x03 bit0=1 family.

Table 7-3. Only existing in DIE_ID Register 0x03 bit0=1 family

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL5 (Only for DIE_ID Register 0x03 bit0=1)	0x0A	Meaning	Reserved						LPM	REG_I2C_TIME_OUT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
LPM			Low power mode(LPM) control register: 0 : disable low power mode function 1 : enable low power mode function for power saving.							
REG_I2C_TIME_OUT			I2C time-out control register: 0 : disable I2C time-out feature 1 : enable I2C time-out feature to prevent from system hangout situation, device will automatically reset I2C to restore communication.							

8 MT6691 Packaging

8.1 Outline Dimensions

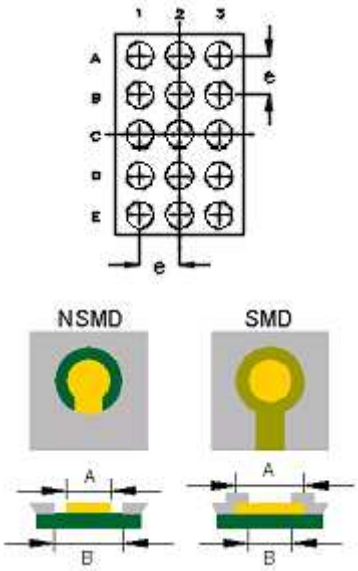


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.980	2.060	0.078	0.081
D1	1.600		0.063	
E	1.270	1.350	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.31x2.02 (BSC)

Figure 8-1. MT6691 Package dimension

8.2 Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.31*2.02-15(BSC)	15	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

Figure 8-2. Footprint information

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