MT6360P Power Management IC
Product Brief

Version: **1.0**
Release date: **2023-09-18**

The full datasheet is available with an NDA

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Version History

Version	Date	Description
1.0	2023-09-18	Official release

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1 Overview

1.1 Features

- **Battery charger**
  - High-accuracy voltage/current regulation
  - Average input current regulation (AICR): 0.1~3.25A in 50 mA steps
  - Charge current regulation accuracy: ±5%
  - Charge voltage regulation accuracy: ±0.5% (0~70°C)
  - Synchronous 1.5 MHz fixed-frequency PWM controller with up to 95% duty cycle
  - Thermal regulation and protection
  - Over-temperature protection
  - Input over-voltage protection
  - IRQ output for communication via I^2C
  - Automatic charging
  - BATFET control to support ship mode, wake-up, and full system reset
  - Resistance compensation from charger output to cell terminal
  - USB OTG output voltage range: 4.85~5.825V
  - D+/D- detection for BC1.2
  - Micro-B ID pin rust
  - Integrated ADCs for system monitoring (charger current, voltage, and temperature)
  - Low battery protection from 2.7V to 3.8V for boost operation
  - Initial VOREG set for relieve battery protection
- **USB_PD**
  - PD-compatible dual-role
  - Attach/Detach detection as host, device or dual-role port
  - Current capability definition and detection
  - Cable recognition
  - Supports alternate mode
  - Supports VCONN with programmable over-current protection (OCP)
  - Supports dead battery
  - Supports BIST mode
  - USB PD3.0
- **Flash LED driver**
  - Synchronous boost dual flash LED driver with dual independently-programmable LED current sources
  - Torch mode current: 25~400 mA in 12.5 mA steps per channel
  - I^2C-programmable flash safety timer, from 64 ms to 2,432 ms with 32 ms/step
  - Flash LED1/LED2 short-circuit protection; output short-circuit protection
  - TXMask protection with dedicated FL_TXMASK pin
  - Shared charger/OTG as power stage
  - Independent torch bypass MOSFET from VSYS

  - Strobe mode current: 50 mA ~ 1.5A in 12.5 mA steps or 25~750 mA in 6.25 mA steps per channel; up to 2.5A in total
- **LDO**
  - 6-channel LDO
  - LDO1 output current: 150 mA
  - LDO2/3 output current: 200 mA
  - LDO5 output current: 800 mA
  - LDO6 output current: 300 mA
  - LDO7 output current: 600 mA
- **RGB LED driver**
  - 3-channel LED driver
  - Sink current for 3 RGB LEDs: 24 mA/channel
  - Flash mode frequency range: 0.125~256 Hz
  - RGB_ISINK1 for CHG_VIN power food indicator
  - Supports register mode, flash mode, breath mode
- **Moonlight LED driver**
  - 5~150 mA sink type LED driver
  - Linear mode control
  - 5 mA/Step
- **Buck**
  - 2-channel buck
  - 0.3~1.3V programmable slew rate for voltage transitions
  - Output current capability: 3A
  - Supports sequenced off delay time selection
  - Input under-voltage lockout (UVLO)
  - Thermal shutdown and overload protection

1.2 Applications

- Cellular telephones
- Personal information appliances
- Tablet PCs
- Portable instruments
- Industrial HMI, desktop POS, KIOSK, digital signage

1.3 General Description

MT6360P is a highly-integrated smart power management IC which includes a single cell Li-Ion/Li-Polymer switching battery charger, a USB Type-C and power delivery (PD) controller, dual flash LED current sources, a RGB LED driver, two buck converters, and six LDOs for portable devices.

The switching charger integrates a synchronous PWM controller, power MOSFETs, input current sensing and input current regulation, high-accuracy voltage regulation, and charge termination circuitry. Besides, the charge current is regulated through the integrated sensing resistors. It also features USB on-the-go (OTG) support.

The USB Type-C and PD controller complies with the latest USB Type-C and PD standards. It integrates a complete Type-C transceiver including the Type-C termination resistors, Rp and Rd, and enables the USB Type-C detection including attach and orientation. It also integrates the physical layer of the USB BMC power delivery protocol, allowing power transfers and role swaps. The BMC PD function provides full support for alternate modes on the USB Type-C standard.

Dual independent current sources supply for each flash LED. The power for the current sources in strobe mode are from the CHG_VMID pin, which is supplied from the charger in reverse boost mode, the same operation as OTG mode of the charger. The high-side current sources, allowing for grounded-cathode connection for LEDs, provide strobe mode current levels from 50 mA to 1.5A in a 12.5 mA step or from 25 mA to 750 mA in a 6.25 mA step, and torch mode current levels from 25 mA to 400 mA in a 12.5mA step. The two channels is able to support totally up to 2.5A.

The dual buck converter delivers a digitally programmable output 0.3V to 1.3V from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I^2C interface capable of operating up to 3.4 MHz.

By using a proprietary architecture with synchronous rectification, BUCK1/2 are capable of delivering 3A continuously as PVIN > 3.1V.

LDO1 supplies power to finger print unit (VFP); LDO2 supplies power to the touch panel unit (VTP); LDO3 and LDO5 supply power to SD card and UFS card (VMC and VMCH); LDO6 and LDO7 supply power to DRAM (VMDDR and VDRAM2). These are in mobile phones and other hand-held devices. The output voltage is programmable via the I^2C interface.

The RGB LED driver is a 3-channel smart LED string controller to drive three channels of LEDs with a sink current of up to 24 mA and a CHG_VIN power good indicator with a sink current of up to 24 mA. All channels can be set independently via the I^2C interface and are provided with three operation modes, register mode, flash mode and breath mode.

MT6360P is available in a WL-CSP-103B 4.64×4.14 (BSC) package.

1.4 Ordering Information

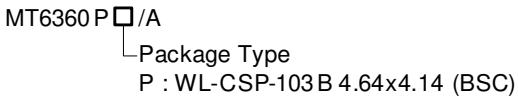


Figure 1-1. Ordering information

1.5 Pin Assignments and Description

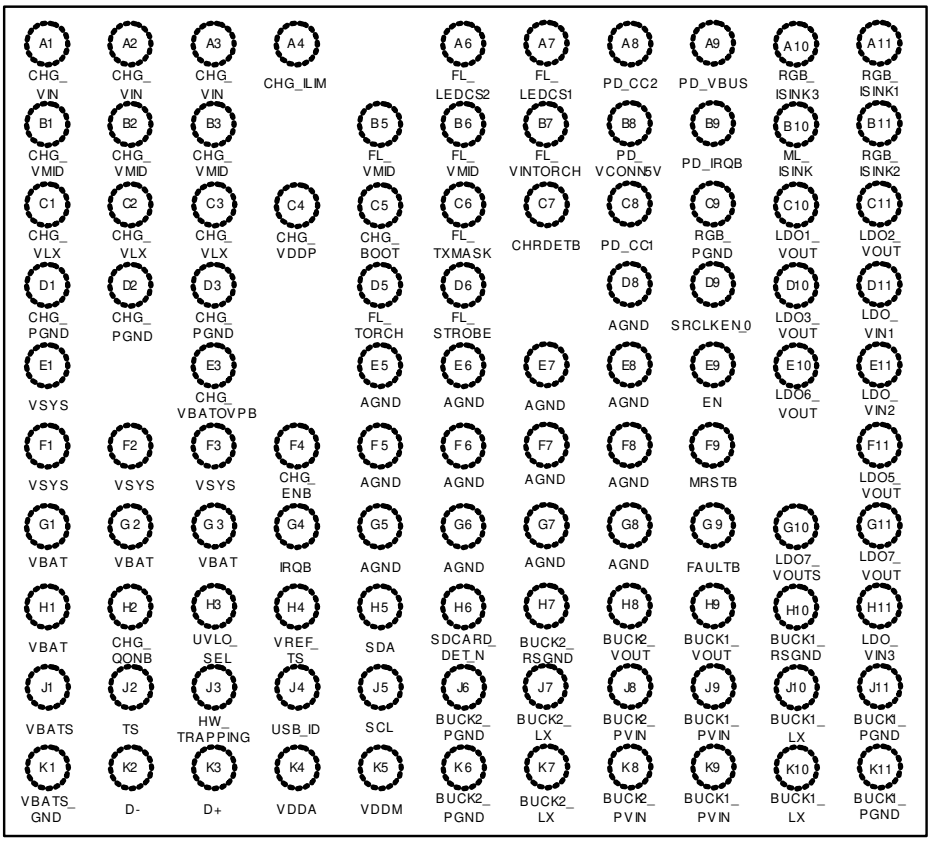


Figure 1-2. MT6360P WL-CSP-103B 4.64×4.14 (BSC) (top view)

Table 1-1. MT6360P pin description

Pin no.	Pin name	Pin description
A1, A2, A3	CHG_VIN	Charger power input
A4	CHG_ILIM	Input current limit setting pin A resistor is connected from CHG_ILIM pin to ground to set up the maximum input current limit. The actual input current limit is the lower value set through the CHG_ILIM pin and IAICR register bits.
A6	FL_LEDCS2	High-side current source output 2 for flash LED2
A7	FL_LEDCS1	High-side current source output 1 for flash LED1
A8	PD_CC2	Type-C connector configuration channel (CC) 2 This is used to detect a cable plug event and determine the cable orientation.
A9	PD_VBUS	CHRDETB detection and VBUS input for attach and detach detection when the device operates as an UFP port
A10	RGB_ISINK3	RGB LED current sink output 3
A11	RGB_ISINK1	RGB LED current sink output 1
B1, B2, B3	CHG_VMID	Connection point between the reverse-blocking MOSFET and the high-side switching MOSFET
B5, B6	FL_VMID	Flash LED driver power input for strobe mode Connect a 4.7µF ceramic capacitor between FL_VMID and ground.
B7	FL_VINTORCH	Flash LED driver power input for torch mode
B8	PD_VCONN5V	Regulated input voltage to power PD_CC pins as VCONN
B9	PD_IRQB	Active-low open-drain interrupt output This requests the processor to check the registers.
B10	ML_ISINK	Moonlight LED current sink output
B11	RGB_ISINK2	RGB LED current sink output 2
C1, C2, C3	CHG_VLX	Charger switch node for output inductor connection
C4	CHG_VDDP	Regulated output voltage to supply for the PWM low-side gate driver and the bootstrap capacitor Connect a 2.2µF ceramic capacitor between CHG_VDDP and ground. 1. If VBUS is plugged in, CHG_VDDP will be powered by CHG_VIN and regulated to 4.9V. 2. If VBUS is unplugged, the charger will operate in sleep mode and the CHG_VDDP voltage will be 0V.
C5	CHG_BOOT	Charger bootstrap voltage to supply the high-side MOSFET gate driver Connect a capacitor between CHG_BOOT and CHG_VLX.
C6	FL_TXMASK	Configurable power amplifier synchronization input or configurable active-high torch mode enable Connect a 300kΩ internal pull-down resistor between FL_TXMASK and ground.
C7	CHRDETB	CHG_VIN ready indication, open-drain output that indicates PD_VBUS is in
C8	PD_CC1	Type-C connector configuration channel (CC) 1 This is used to detect a cable plug event and determine the cable orientation.
C9	RGB_PGND	RGB ground Tie RGB_PGND and ground on the PCB.
C10	LDO1_VOUT	LDO1 output
C11	LDO2_VOUT	LDO2 output
D1, D2, D3	CHG_PGND	Charger ground

Pin no.	Pin name	Pin description
		Tie CHG_PGND and ground on the PCB.
D5	FL_TORCH	Flash LED torch mode enable input
D6	FL_STROBE	Flash LED strobe mode enable input
D8, E5, E6, E7, E8, F5, F6, F7, F8, G5, G6, G7, G8	AGND	Analog ground Tie AGND and ground on the PCB.
D9	SRCLKEN_0	Source clock enable on and LP control pin 0
D10	LDO3_VOUT	LDO3 output
D11	LDO_VIN1	LDO_VIN1 power input for LDO1, LDO2 and LDO3 Connect a 2.2µF ceramic capacitor between LDO_VIN1 and ground.
E1, F1, F2, F3	VSYS	System connection node Internal BATFET is connected between VSYS and VBAT. Connect a 22µF ceramic capacitor between VSYS and ground.
E3	CHG_VBATOVPB	Battery over-voltage protection (BAT OVP) indication This is an open-drain and active-low output. It will be low if BAT OVP occurs; otherwise, it is high.
E9	EN	BUCK1, BUCK2, LDO6 and LDO7 enable control input When EN = low, all bucks and LDOs are turned off.
E10	LDO6_VOUT	LDO6 output
E11	LDO_VIN2	LDO_VIN2 power input for LDO5 and logic circuit of LDO6/7 Connect a 2.2µF ceramic capacitor between LDO_VIN2 and ground.
F4	CHG_ENB	Charger enable input, active-low
F9	MRSTB	Manual reset input for hardware reset
F11	LDO5_VOUT	LDO5 output
G1, G2, G3, H1	VBAT	Charge current output node for battery connection The internal BATFET is connected between VSYS and VBAT. Connect a 10µF ceramic capacitor between VBAT and ground.
G4	IRQB	Active-low open-drain interrupt output This requests the processor to read the registers.
G9	FAULTB	Indicates power not good of bucks and LDOs Active-low open-drain
G10	LDO7_VOUTS	LDO7 output voltage-sense input
G11	LDO7_VOUT	LDO7 output
H2	CHG_QONB	Internal BATFET enable control input In shipping mode, CHG_QONB is pulled low for the duration of tSHIPMODE_CHG (typical 0.9s) to exit shipping mode.
H3	UVLO_SEL	SYSUVLO rising threshold voltage setting and the UVLO_SEL pin defines default value
H4	VREF_TS	Power output of 1.8V reference power for temperature sensing
H5	SDA	I^2C interface serial data input/output Open-drain. An external pull-up resistor is required.
H6	SDCARD_DET_N	When SDCARD_DET_N is active, disable LDO5.
H7	BUCK2_RSGND	BUCK2 remote sense ground
H8	BUCK2_VOUT	BUCK2 output voltage sense through this pin
H9	BUCK1_VOUT	BUCK1 output voltage sense through this pin
H10	BUCK1_RSGND	BUCK1 remote sense ground
H11	LDO_VIN3	LDO_VIN3 power input for LDO6 and LDO7 Connect a 2.2µF ceramic capacitor between LDO_VIN3 and ground.
J1	VBATS	Battery voltage-sense

Pin no.	Pin name	Pin description
J2	TS	Temperature-sense input, connected to a resistor divider for temperature programming
J3	HW_TRAPPING	Either uses an external pull-down resistor or connects the pin to VDDA to define power configuration
J4	USB_ID	USB ID port connected to USB receptacle
J5	SCL	I^2C interface serial clock input Open-drain. An external pull-up resistor is required.
J6, K6	BUCK2_PGND	BUCK2 power ground The low-side MOSFET is referenced to this pin. CIN and COUT should be returned with a minimal path to these pins.
J7, K7	BUCK2_LX	BUCK2 switching node Connect to the inductor.
J8, K8	BUCK2_PVIN	BUCK2 power input voltage Connect to the input power source. Connect to CIN with minimal path.
J9, K9	BUCK1_PVIN	BUCK1 power input voltage Connect to the input power source. Connect to CIN with minimal path.
J10, K10	BUCK1_LX	BUCK1 switching node Connect to the inductor.
J11, K11	BUCK1_PGND	BUCK1 power ground The low-side MOSFET is referenced to this pin. CIN and COUT should be returned with a minimal path to these pins.
K1	VBATS_GND	Battery voltage-sense ground
K2	D-	USB D- port
K3	D+	USB D+ port
K4	VDDA	Regulated power input for an internal analog base Connect a 2.2µF ceramic capacitor between VDDA and ground.
K5	VDDM	Regulated voltage output Connect a 2.2µF ceramic capacitor between VDDM and PGND. It also provides power to all VDDA-powered circuits.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1. Absolute maximum ratings

(1)

Parameter	Condition	Min.	Typ.	Max.	Unit
PD_VBUS		-0.5	-	28	V
PD_CC1, PD_CC2		-0.5	-	24	V
Battery pin input (4)	Steady state	-0.5	-	6	V
	Transient (< 10 ms)	-0.5	-	7	V
CHG_VIN, CHG_VMID, CHG_BOOT, FL_VMID		-0.5	-	22	V
USB ID, D+, D-		-0.5	-	24	V
CHG_LX		-0.5	-	16	V
	LX (peak < 100 ns duration)	-	-	-2	
Other pins		-0.5	-	6	V
Power dissipation, P_D	@TA = 25°C WL-CSP-103B 4.64x4.14 (BSC)	-	-	4.44	W
Package thermal resistance (2)	WL-CSP-103B 4.64x4.14 (BSC), θ_{JA}	-	22.5	-	°C/W
Lead temperature	Soldering, 10 sec.	-	-	260	°C
Storage temperature range		-65	-	150	°C
ESD susceptibility (3)	HBM (human body model)	-	-	2	kV

(1) Note 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

(2) Note 2 θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

(3) Note 3 Devices are ESD sensitive. Handling precaution is recommended.

(4) Note 4 Battery input pin: VBAT/VBATS/VSYS/BUCKx_PVIN/BUCKx_LX/LDO_VINx/FL_VINTORCH

2.2 Recommended Operating Range

- PD_VBUS, CHG_VIN supply input voltage: 4~14V
- VBAT supply input voltage: 2.8~5V
- BUCK1/2_PVIN input voltage: 3.1~5V
- LDO_VIN1/2: 3.15~5V
- LDO_VIN3: 1.1~5V
- IBAT (discharging current with internal MOSFET): 6A (continues)
- IBAT (discharging current with internal MOSFET): 9A (peak, up to 1 sec duration)
- Junction temperature range: -40~125°C
- Ambient temperature range: -40~85°C

Note. The device is not guaranteed to function outside its operating conditions.

2.3 Electrical Characteristics

V_{CHG_VIN} = 5V, V_{BAT} = 4.2V, L1 = L2 = 0.33µH, L3 = 1µH, C2 = 2.2µF, C18 = 10µF, T_A = 25°C, unless otherwise specified

Table 2-2. Electrical specifications

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
PMIC quiescent current						
Shutdown current	I_{SHDN}	On VBAT pin, with all channels shut down, V_{BAT} = 4V	-	63	85	µA
Shipping-mode current	I_{BAT_SHIP}	VBAT only, in shipping mode	-	16	40	µA
CHG_VIN supply current	I_{CHG_VIN}	V_{CHG_VLX} is non-switching V_{CHG_VIN} = 5V, V_{BAT} = V_{CV_CHG} ICHG = 0 Flash LED, LDOs, bucks and RGB devices disabled, PD cable attached (Full functions are not in the communication situation.)	-	4.6	6.8	mA
CHG_VIN supply current with charger in H-Z mode	$I_{CHG\_VIN\_HZ}$	V_{CHG_VLX} is in high-impedance mode V_{CHG_VIN} = 5V, V_{BAT} =4V Flash LED, LDOs, bucks, PD and RGB devices disabled	-	210	500	µA
Over-temperature protection threshold	T_{OTP}	Thermal shutdown threshold temperature	-	150	-	°C
Over-temperature protection accuracy	T_{OTP_ACC}	Thermal shutdown temperature accuracy	-15	-	15	°C
Over-temperature protection recover	$T_{OTP\_RECOVER}$	Thermal shutdown recover temperature	95	110	125	°C
Control I/O pin, VDDA and VSYS						
Logic-low threshold voltage for all open-drain outputs	V_{OL}	I_{DS} = 10 mA	-	-	0.4	V
Logic-high threshold voltage for all inputs	V_{IH}	Logic-high threshold	1.2	-	-	V
Logic-low threshold voltage for all inputs	V_{IL}	Logic-low threshold	-	-	0.4	V
SYS under-voltage protection rising threshold range	$V_{SYS\_UVLO\_RISE}$	External R selection R = 1 MΩ (2.9V), 100 mV/step	2.8	-	3.3	V
SYS under-voltage protection rising threshold accuracy	$V_{SYS\_UVLO\_ACC\_RISE}$	V_{SYS} rising, default 2.9V	-50	-	+50	mV
De-bouncing time by SYS UVLO rising	$t_{DEBOUN\_SYS\_UVLO\_RISE}$		-	15	-	ms
SYS under-voltage protection falling threshold range	$V_{SYS\_UVLO\_FALL}$	I^2C programmable, default 2.5V, 50 mV/step	2.4	-	2.8	V
SYS under-voltage protection falling threshold accuracy	$V_{SYS\_UVLO\_ACC\_FALL}$	V_{SYS} falling, default 2.5V	-50	-	+50	mV
VDDA over-voltage protection threshold	V_{VDDA_OVP}	V_{DDA} rising	5.25	5.5	5.75	V

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
VDDA over-voltage protection hysteresis	$V_{VDDA\_OVP\_HYS}$	V_{DDA} falling	-	0.2	-	V
Pull-down ability on MRSTB	I_{PD_MRSTB}		-	1	2.3	µA
Pull-down ability on SDCARD_DET_N	$I_{PD\_SDCARD\_DET\_N}$		-	1	2.3	µA
Pull-down resistance on SRCLKEN_0	$R_{SRCLKEN\_0}$		-	1	2.3	µA
Pull-down resistance on EN	R_{EN}		-	350	-	kΩ
USB ID						
USB_ID pull-up voltage	$V_{USB\_ID\_PULLUP}$	V_{USB_ID} = 0.6V, 0x6F[7] = 1	0.57	0.6	0.63	V
		V_{USB_ID} = 1.8V, 0x6F[7] = 0	1.71	1.8	1.89	V
USB_ID pull-up resistance tolerance	$R_{USB\_ID\_PULLUP}$	500 kΩ, 75 kΩ, 5 kΩ, 1 kΩ	-20	-	20	%
USB_ID pull-down resistance	$R_{USB\_ID\_PULLUP}$	500 kΩ, 75 kΩ, 5 kΩ, 1 kΩ	3.75	5	6.25	kΩ
Interrupt threshold voltage	V_{ID_INT}	0x6F[6] = 0, 0x6F[7] = 0	1.3	1.45	1.6	V
		0x6F[6] = 1, 0x6F[7] = 1	0.18	0.2	0.22	
Interrupt threshold voltage hysteresis	$V_{ID\_INT\_HYS}$	0x6F[7] = 1	-	0.05	-	V
		0x6F[7] = 0	-	0.1	-	
Interrupt debounce time tolerance	$t_{ID\_INT\_DEB}$	I^2C programmable,5 µs ~ 64 ms (default 50 µs)	-10	-	10	%
Input equivalent capacitance	$C_{ID\_IN\_CAP}$		-	-	20	pF
Charger						
Sleep-mode entry threshold	$V_{SLEEP\_ENTER\_CHG}$	V_{CHG_VIN} falling, V_{CHG_VIN} - V_{BAT}	0	0.04	0.1	V
Sleep-mode exit threshold	$V_{SLEEP\_EXIT\_CHG}$	V_{CHG_VIN} rising, V_{CHG_VIN} - V_{BAT}	0.04	0.1	0.2	V
Sleep-mode exit deglitch time	$t_{D\_SLEEP\_EXIT\_CHG}$	Exit sleep-mode	-	120	-	ms
CHG_VIN bad adapter threshold	$V_{BAD\_ADP\_CHG}$	V_{CHG_VIN} falling	-	3.8	-	V
CHG_VIN bad adapter hysteresis	$V_{BAD\_ADP\_HYS\_CHG}$	V_{CHG_VIN} rising	-	150	-	mV
CHG_VIN bad adapter sink current	$I_{BAD\_ADP\_SINK\_CHG}$		-	50	-	mA
CHG_VIN bad adapter detection time	$t_{BAD\_ADP\_DET\_CHG}$		-	30	-	ms
Input current limit factor	K_{ILIM_CHG}	Input current regulation 508 mA by CHG_ILIM pin with resistance = 698Ω	320	355	390	AΩ
CHG_VIN minimum input voltage regulation (MIVR) threshold	V_{MIVR_CHG}	I^2C programmable range in 0.1V steps	3.9	-	13.4	V
CHG_VIN minimum input voltage regulation accuracy	$V_{MIVR\_ACC\_CHG}$	V_{MIVR} = 4.4V or 9V	-2	-	2	%
AICR 100 mA mode	$I_{AICR\_100mA\_CHG}$	I_{AICR} = 100 mA, V_{CHG_VIN} = 5V, V_{BAT} = 3.8V	86	93	100	mA

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
AICR 500 mA mode	$I_{AICR\_500mA\_CHG}$	I_{AICR} = 500 mA, V_{CHG_VIN} = 5V, V_{BAT} = 3.8V	440	470	500	mA
AICR 1,000 mA mode	$I_{AICR\_1000mA\_CHG}$	I_{AICR} = 1,000 mA, V_{CHG_VIN} = 5V, V_{BAT} = 3.8V	880	940	1,000	mA
AICR 1,500 mA mode	$I_{AICR\_1500mA\_CHG}$	I_{AICR} = 1,500 mA, V_{CHG_VIN} = 5V, V_{BAT} = 3.8V	1,300	1,400	1,500	mA
CHG_VIN UVLO	V_{UVLO_CHG}	V_{CHG_VIN} rising	3.05	3.3	3.55	V
CHG_VIN UVLO hysteresis	$V_{UVLO\_HYS\_CHG}$	V_{CHG_VIN} falling	-	150	-	mV
CHG_VIN over-voltage protection threshold	$V_{CHG\_VIN\_OVP\_CHG1}$	V_{CHG_VIN} rising, I^2C programmable 5.5V	5.17	5.5	5.86	V
CHG_VIN over-voltage protection threshold	$V_{CHG\_VIN\_OVP\_CHG2}$	V_{CHG_VIN} rising, I^2C programmable 6.5V (default)	6.11	6.5	6.92	V
CHG_VIN over-voltage protection threshold	$V_{CHG\_VIN\_OVP\_CHG3}$	V_{CHG_VIN} rising, I^2C programmable 11V	10.34	11	11.71	V
CHG_VIN over-voltage protection threshold	$V_{CHG\_VIN\_OVP\_CHG4}$	V_{CHG_VIN} rising, I^2C programmable 14.5V	13.63	14.5	15.44	V
CHG_VIN over-voltage protection propagation delay	$t_{CHG\_VIN\_OVP\_CH}$	V_{CHG_VIN} rising above V_{CHG_VIN} over-voltage protection threshold turn off UUG MOS, OVP setting = 6.5V	-	100	-	ns
CHG_VIN over-voltage protection hysteresis	$V_{CHG\_VIN\_OVP\_HYS\_CHG}$	V_{CHG_VIN} falling	-	250	-	mV
VBAT over-voltage protection threshold	$V_{BAT\_OVP\_CHG}$	V_{BAT} rising, as percentage of V_{OREG_CHG}, as V_{BAT}/V_{OREG_CHG}, 0x12[4] TE = 0	106	108	110	%
VBAT over-voltage protection hysteresis	$V_{BAT\_OVP\_HYS\_CHG}$	V_{BAT} falling, as (V_{BAT} - V_{OREG_CHG})/V_{OREG_CHG} 0x12[4] TE = 0	-	2	-	%
Thermal regulation threshold	T_{THREG_CHG}	Charge current starts decreasing (default)	-	120	-	°C
VSYS over-voltage protection threshold	$V_{SYS\_OVP\_CHG}$	V_{SYS} rising	4.9	5.25	5.5	V
VSYS under-voltage protection threshold	$V_{SYS\_UVP\_CHG}$	V_{SYS} falling	2.2	2.4	2.6	V
VBAT depletion threshold voltage	$V_{BAT\_DPL\_RISE}$	V_{BAT_DPL} rising	2.3	2.5	2.8	V
VBAT depletion threshold voltage	$V_{BAT\_DPL\_FALL}$	V_{BAT_DPL} falling	2	2.3	2.39	V
CHG_VIN force sleep mode supply current	$I_{CHG\_VIN\_SLEEP}$	Reg: 0x11[3] = 1	-	-	2.5	mA
End of charge						
Battery regulation voltage range	V_{OREG_CHG}	I^2C programmable in 10 mV steps	3.9	-	4.71	V
Battery regulation voltage accuracy	$V_{OREG\_ACC\_CHG}$	V_{OREG_CHG} = 4.2V, 4.35V, 4.36V, 4.37V, 4.38V, 4.43V or V_{OREG_CHG} = 4.45V (T_C = -10~ 70°C) (3)	-0.5	-	0.5	%
Re-charge mode threshold	V_{RECH_CHG}	I^2C programmable, V_{BAT} falling, difference below V_{OREG_CHG}	50	100	150	mV
Re-charge deglitch time	$t_{D\_RECH\_CHG}$	V_{BAT} falling	-	120	-	ms
End-of-charge current	I_{EOC_CHG}	I^2C programmable in 50 mA steps	100	-	850	mA

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Default end-of-charge current	$I_{EOC\_DEF\_CHG}$	Default	-	250	-	mA
End-of-charge current accuracy	I_{EOC_ACC}	I_{EOC_CHG} = 150 mA, 200 mA, 250 mA	-20	-	20	%
End-of-charge deglitch time	$t_{D\_EOC\_CHG}$		-	2	-	ms
Charge current	I_{CHG}	I^2C programmable in 0.1A steps, 0x17 bit[7:2]	0.3	-	3	A
ICHG current Accuracy 1	$I_{CHG\_ACC1\_CHG}$	V_{BAT} = 3.8V, 300 mA ≤ I_{CHG} < 500 mA, (T_C = -10~70°C)	-20	-	20	%
ICHG current Accuracy 2	$I_{CHG\_ACC2\_CHG}$	V_{BAT} = 3.8V, 500 mA ≤ I_{CHG} < 1,000 mA, (T_C = -10~70°C)	-10	-	10	%
ICHG current Accuracy 3	$I_{CHG\_ACC3\_CHG}$	V_{BAT} = 3.8V, I_{CHG} ≥ 1,000 mA (T_C = -10~70°C)	-5	-	5	%
Pre-charge mode threshold	V_{PRECHG_CHG}	I^2C programmable in 0.1V steps, V_{BAT} rising	2.0	-	3.5	V
Pre-charge mode hysteresis	$V_{PRECHG\_HYS\_CHG}$	Pre-charge hysteresis V_{BAT} falling	-	0.2	-	V
Pre-charge threshold accuracy	$V_{PRECHG\_ACC\_CHG}$		-5	-	5	%
Pre-charge current	I_{PRECHG_CHG}	I^2C programmable (default)	-	150	-	mA
Pre-charge current accuracy	$I_{PRECHG\_ACC\_CHG}$		-20	-	20	%
Trickle charge threshold	V_{TRICHG}	V_{BAT} falling	-	2	-	V
Trickle charge threshold hysteresis	V_{TRICHG_HYS}	V_{BAT} rising	-	200	-	mV
Trickle charge threshold accuracy	V_{TRICHG_ACC}		-5	-	5	%
Trickle current	I_{TRICHG}		-	100	-	mA
Trickle current accuracy	I_{TRICHG_ACC}		-20	-	20	%
VSYS regulation voltage	$V_{SYS\_MIN\_CHG}$	I^2C programmable in 0.1V steps	3.3	-	4	V
VSYS regulation voltage accuracy	$V_{SYS\_MIN\_ACC\_CHG}$		-3	-	3	%
UUG on-resistance	$R_{ON\_UUG\_CHG}$	From CHG_VIN to CHG_VMID	-	10	30	mΩ
UG on-resistance	$R_{ON\_UG\_CHG}$	From CHG_VMID to CHG_VLX	-	20	40	mΩ
LG on-resistance	$R_{ON\_LG\_CHG}$	From CHG_VLX to PGND	-	20	40	mΩ
PPMOS on-resistance	$R_{ON\_PPMOS\_CHG}$	From VSYS to VBAT	-	12	30	mΩ
Switching frequency	f_{OSC0_CHG}	I^2C programmable to 1.5 MHz (default)	-	1.5	-	MHz
Switching frequency accuracy	$f_{OSC\_ACC\_CHG}$		-10	-	10	%
Maximum duty cycle	D_{MAX_CHG}		-	97	-	%
Minimum duty cycle	D_{MIN_CHG}		0	-	-	%
VDDP regulation	V_{VDDP_CHG}	V_{CHG_VIN} = 5.5V	4.5	4.9	5.3	V
Charger buck OCP current	$I_{CHG\_BUCK\_OCP\_CHG}$	REG0x1D[2] = 1'b0	4	6	8	A
		REG0x1D[2] = 1 'b1	5.6	8	10.4	
Internal QONB pull-up resistance	R_{QONB_CHG}		16.15	19	21.85	kΩ

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
QONB exit shipping mode duration	$t_{SHIPMODE\_CHG}$	CHG_QONB low for BATFET on-time to exit shipping mode	0.86	0.96	1.06	s
QONB system reset duration	$t_{QONB\_RST\_CHG}$	CHG_QONB low time to enable full system reset	12	15	18	s
BATFET reset time	$t_{BATFET\_RST\_CHG}$	BATFET off-time during full system reset	0.6	0.66	0.72	s
Shipping mode entry deglitch time	$t_{D\_SHIP\_ENTER}$	Enter shipping mode delay	15	18	21.6	s
AICC threshold	V_{AICC_VTH}	V_{CHG_VIN} rising I^2C programmable	-	4.6	-	V
AICC hysteresis	$V_{AICC\_HYS\_VTH}$		-	50	-	mV
OTG output regulation	V_{BSTCV_CHG}	I^2C programmable default	-	5.05	-	V
OTG output accuracy	$V_{BSTCV\_ACC\_CHG}$	I_{LOAD} = 0 mA	-3	-	3	%
OTG over-load protection threshold	$I_{BST\_0.5A\_CHG}$	OTG_OC = 0.5A REG 0x1A[2:0] = 000	0.5	-	-	A
OTG CHG_VMID over-voltage protection threshold	$V_{MIDOVP\_OTG\_CHG}$	V_{CHG_VMID} rising	5.72	6	6.28	V
OTG CHG_VMID over-voltage protection hysteresis	$V_{MIDOVP\_OTG\_HYS\_CHG}$		-	200	-	mV
OTG VBAT under-voltage protection threshold	$V_{BAT\_UVP\_OTG\_CHG}$	I^2C default, V_{BAT} falling	2.62	2.8	2.98	V
OTG VBAT under-voltage protection hysteresis	$V_{BAT\_UVP\_OTG\_HYS\_CHG}$	V_{BAT} rising	-	400	-	mV
Boost supply current	I_{BOOST_SUPPLY}	OTG mode, I_{LOAD} = 0 mA	-	8	-	mA
OTG over-current protection threshold	$I_{OTG\_OCP\_CHG}$	Default = 6.5A	5.2	6.5	8.2	A
Pull-down ability on CHG_ENB	$I_{PD\_CHG\_ENB}$		-	1	2.3	µA
D+/D- detection						
D+ source voltage	V_{DP_SRC}		0.5	0.6	0.7	V
Data detect voltage	V_{DAT_REF}		0.25	0.3	0.4	V
VLGC voltage	V_{LGC_CHG}		0.8	-	2	V
D- sink current	I_{DM_SINK}		50	100	150	µA
Data contract detect current source	I_{DP_SRC}		7	-	13	µA
Dedicated charging port resistance across D+/-	R_{D+D-_DCP}	sEN_DCP = 1	50	90	130	Ω
D+ source on-time	$t_{DP\_SRC\_ON}$		40	64	-	ms
DCD timeout	$t_{DCD\_TIMEOUT}$		300	-	1,200	ms
D+ source off to high current	t_{DPSRC_HICRNT}		28	32	36	ms
Charger detect debounce	$t_{CHGR\_DET\_DBNC}$		27	30	33	ms
CHRDETB						

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
PD_VBUS over-voltage protection threshold range	$V_{PD\_VBUS\_OVP}$	$V_{PD\_VUS\_OVP}$ rising, I^2C programmable (default 10.5V)	6	-	14.5	V
PD_VBUS over-voltage protection accuracy	$V_{PD\_VBUS\_OVP\_ACC}$		-3	-	3	%
PD_VBUS over-voltage protection hysteresis	$V_{PD\_VBUS\_HYS}$		-	150	-	mV
PD_VBUS UVLO protection threshold range	$V_{PD\_VBUS\_UVLO}$	$V_{PD\_VUS\_UVLO}$ falling, I^2C programmable 0.1V/Step (default 3.7V)	2.6	-	3.7	V
PD_VBUS UVLO protection accuracy	$V_{PD\_VBUS\_UVLO\_ACC}$		-4	-	4	%
PD_VBUS UVLO protection hysteresis	$V_{PD\_VBUS\_UVLO\_HYS\_}$		-	150	-	mV
ADC						
ADC conversion time	t_{CONV_ADC}	Only for one channel, 0x56[5:3] = 0 ms of waiting time and 0x58[7:0] = 0 ms of idle time	20.8	26	31.2	ms
Number of bits for ADC resolution	R_{ES_ADC}		-	12	-	bit
CHG_VIN_DIV5 measurement range	$V_{VBUS\_DIV5\_ADC\_RANGE}$		1	-	22	V
CHG_VIN_DIV5 resolution	$V_{VBUS\_DIV5ADC\_RES}$		-	25	-	mV
CHG_VIN_DIV5 accuracy	$V_{VBUS\_DIV5ADC\_ACC}$		-3	-	3	LSB
CHG_VIN_DIV2 measurement range	$V_{VBUS\_DIV2\_ADC\_RANGE}$		1	-	VDDA*2	V
CHG_VIN_DIV2 resolution	$V_{VBUS\_DIV2ADC\_RES}$		-	10	-	mV
CHG_VIN_DIV2 accuracy	$V_{VBUS\_DIV2ADC\_ACC}$		-3	-	3	LSB
VBAT measurement range	$V_{BAT\_ADC\_RANGE}$		0	-	VDDA	V
VBAT resolution	$V_{BAT\_ADC\_RES}$		-	5	-	mV
VBAT accuracy	$V_{BAT\_ADC\_ACC}$		-3	-	3	LSB
VSYS measurement range	$V_{SYS\_ADC\_RANGE}$		0	-	VDDA	V
VSYS resolution	$V_{SYS\_ADC\_RES}$		-	5	-	mV
VSYS accuracy	$V_{SYS\_ADC\_ACC}$		-3	-	3	LSB
IBUS measurement range	$I_{IBUS\_ADC\_RANGE}$		0	-	5	A
IBUS resolution	$I_{IBUS\_ADC\_RES}$		-	50	-	mA
IBUS accuracy	$I_{IBUS\_ADC\_ACC}$	I_{BUS} > 2A, IAICR [7:2] setting ≥ 400 mA	-3	-	3	LSB
		I_{BUS} < 2A, IAICR [7:2] setting ≥ 400 mA	-2	-	2	
		I_{BUS} < 2A, IAICR [7:2] setting < 400 mA	-2	-	2	
IBAT measurement range	$I_{IBAT\_ADC\_RANGE}$		0	-	5	A

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
IBAT resolution	$I_{IBAT\_ADC\_RES}$		-	50	-	mA
IBAT accuracy	$I_{IBAT\_ADC\_ACC}$		-2	-	2	LSB
TEMP_JC measurement range	$T_{TEMP\_JC\_ADC\_RANGE}$		-40	-	120	°C
TEMP_JC resolution	$T_{TEMP\_JC\_ADC\_RES}$		-	2	-	°C
TEMP_JC accuracy	$T_{TEMP\_JC\_ADC\_ACC}$	Temperature < 85°C	-3	-	3	LSB
VREF_TS pull-up voltage	$V_{REF\_TS\_ADC}$		1.782	1.8	1.818	V
TS voltage measurement range	$V_{TS\_ADC\_RANGE}$		0	-	VDDA	V
TS resolution	$V_{TS\_ADC\_RES}$		-	5	-	mV
TS accuracy	$T_{TS\_ADC\_ACC}$		-2	-	2	LSB
USB_ID measurement range	$V_{USBID\_ADC\_RANGE}$	VDDA > 3.4V	0	-	VDDA - 1.4	V
USB_ID resolution	$V_{USB\_ID\_ADC\_RES}$		-	5	-	mV
Pump express						
PE+1 on time (A)	$t_{ON\_A\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	430	500	570	ms
PE+1 on time (B)	$t_{ON\_B\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	240	300	360	ms
PE+1 on time (C)	$t_{ON\_C\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	70	100	130	ms
PE+1 off time (D)	$t_{OFF\_D\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	70	100	130	ms
PE+1 off time (I)	$t_{OFF\_I\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	80	-	225	ms
PE+2 off time (D)	$t_{OFF\_D\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	87	105	128	ms
PE+2 on time (E)	$t_{ON\_E\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	147	190	248	ms
PE+2 on time (F)	$t_{ON\_F\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	87	102.5	118	ms
PE+2 on time (G)	$t_{ON\_G\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	22	50	68	ms
PE+2 off time (H)	$t_{OFF\_H\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	22	50	68	ms
PE+2 off time (I)	$t_{OFF\_I\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	135	155	175	ms
Flash LED current source						
LED current accuracy	$I_{LED\_ACC\_FL}$	Flash LED current can be set from 25 mA to 400 mA	-8	-	8	%
LED current accuracy	$I_{LED\_ACC\_FL}$	Flash LED current can be set from 0.4A to 1.5A	-6	-	6	%
FL_LEDCSx leakage current	I_{LEAK_FL}	VLEDVIN = 5V, LEDCSX = 0, LEDCSX is disabled	-	0.1	4	µA
FL_LEDCSx start-up current	I_{START_FL}	LEDCSX = 0, LEDCSX is enabled	-	320	1,000	µA
LEDCSX short threshold	V_{SC_FL}		-	1	1.3	V
LEDCSX short event timer	$t_{D\_SC\_FL}$		1.8	2.5	3.3	ms
Flash timeout	$t_{TIMEOUT\_FL}$	FLEDx_STRB_TO = 0100101	-	1,248	-	ms
Flash timer accuracy	$t_{TMR\_ACC\_FL}$	Timer is set by register.	-10	-	10	%
Current source regulation voltage	V_{REG_FL}	I_{LED} = 200 mA, 0x7C[1:0] = 00	-	200	300	mV
Current source regulation voltage	V_{REG_FL}	I_{LED} = 1,500 mA, 0x7C[1:0] = 01	-	-	500	mV
Strobe/TXMask deglitch time	$t_{D\_STRB\_FL}$		-	10	-	µs
Flash ready time	$t_{FLSH\_RDY\_FL}$	EN_LEDCS = 1 to current reach 800 mA target value	-	4.5	5	ms

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Strobe FL-CHG_VIN OVP	$V_{IN\_OVP\_FL}$		5.45	5.6	5.75	V
Strobe FL-CHG_VIN OVP hysteresis	$V_{IN\_OVP\_Hys\_FL}$		0.23	0.3	0.37	V
High-side switch on-resistance	$R_{ON\_H\_FL}$		-	60	-	mΩ
Low-side switch on-resistance	$R_{ON\_L\_FL}$		-	36	-	mΩ
Pull-down resistance on FL_STROBE	$R_{L\_FL\_STROBE}$		-	350	-	kΩ
Pull-down resistance on BL_EN	$R_{L\_FL\_TORCH}$		-	350	-	kΩ
Pull-down resistance on FL_TXMASK	$R_{L\_FL\_TXMASK}$		-	350	-	kΩ
USB_PD						
Bit rate	$f_{BitRate\_PD}$		270	300	330	Kbps
Maximum difference between the bit rate during the part of the packet following the preamble and the reference bit-rate	$p_{BitRate\_PD}$		-	-	0.25	%
Time from the end of last bit of a frame until the start of the first bit of the next preamble	$t_{InterFrameGap\_PD}$		25	-	-	µs
Time before the start of the first bit of the preamble when the transmitter should start driving the line	$t_{StartDrive\_PD}$		-1	-	1	µs
Time to cease driving the line after the end of the last bit of the frame	$t_{EndDriveBMC\_PD}$		-	-	23	µs
Falling time	t_{Fall_PD}		300	-	-	ns
Time to cease driving the line after the final high-to-low transition	$t_{HoldLowBMC\_PD}$		1	-	-	µs
Rising time	t_{Rise_PD}		300	-	-	ns
Voltage swing	V_{Swing_PD}		1.05	1.125	1.2	V
Transmitter output impedance	z_{Driver_PD}		33	-	75	Ω
Time window for detecting non-idle	$t_{TransitionWindow\_PD}$		12	-	20	µs
Receiver input impedance	z_{BmcRx_PD}		1	-	-	MΩ
Low-power mode	$I_{LOW\text{-}POWER\_PD}$	DRP toggle	-	32	45	µA
VCONN switch on-resistance	$R_{ON\_VCONN\_PD}$		-	0.7	1	Ω
OCP range	I_{OCP_PD}		200	-	600	mA
DFP 80µA CC current	$I_{CC\_DFP80µ\_PD}$		64	80	96	µA

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
DFP 180µA CC current	$I_{CC\_DFP180µ\_PD}$		166	180	194	µA
DFP 330µA CC current	$I_{CC\_DFP330µ\_PD}$		304	330	356	µA
UFP pull-down resistance through CC pin	$Rd_{\_PD}$		4.59	5.1	5.61	kΩ
UFP pull-down threshold voltage in dead battery	$V_{TH\_DBL\_PD}$	Under I_{CHG} = $I_{CC\_DFP80µ\_PD}$ and $I_{CC\_DFP180µ\_PD}$	0.2	-	1.6	V
UFP pull-down threshold voltage in dead battery	$V_{TH\_DBH\_PD}$	Under I_{CHG} = $I_{CC\_DFP330µ\_PD}$	0.8	-	2.45	V
Valid VBUS detection threshold	$V_{VALID\_VBUS\_PD}$		3.5	-	4.0	V
CC pin lower pull-up voltage	$V_{LPWR\_PULLUP\_CC}$	REG 0xAB bit = 0 in low-power mode	1.8	2	2.2	V
RGB/Moonlight LED driver						
Current accuracy	$I_{LED\_ACC\_RGB}$	I_{LED} = 20 mA	-5	-	5	%
Current matching	$I_{LED\_MATCH\_RGB}$	I_{LED} = 20 mA	-5	-	5	%
Dropout voltage	V_{DROP_RGB}	I_{LED} = 20 mA	-	75	150	mV
RGB_ISINK1/2/3 output current range	I_{LED_ISINK}		1	-	24	mA
Moonlight output current range	I_{LED_ML}	5 mA/step	5	-	150	mA
Moonlight current accuracy	$I_{LED\_ACC\_ML}$	I_{LED} = 60 mA (default)	-5	-	5	%
Moonlight dropout voltage	$V_{ML\_DROP\_RGB}$	I_{LED} = 150 mA	-	-	200	mV
RGB supply current	$I_{LED\_ISINK\_SUPPLY}$	All 3 channels set to 20 mA	-	203	-	µA
		2 channels set to 20 mA	-	162	-	µA
		1 channels set to 20 mA	-	122	-	µA
Moonlight supply current	$I_{LED\_ML\_SUPPLY}$	Moonlight set to 100 mA	-	176	-	µA
RGB timing accuracy	T_{ACC_RGB}		-5	-	5	%
BUCK1						
Turn-on overshoot		VOUT = default, no load	-	-	10	%
Over-current protection (OCP)	I_{OCP1}	Peak inductor current, as REG_PMIC, 0x15[2:1] = 01	4	5	6	A
Efficiency	$Eff_{\_BUCK}$	VBAT = 4V, Vout = 0.8V, I_LOAD = 100 mA, L_DCR_max = 26 mΩ	-	84	-	%
		VBAT = 4V, Vout = 0.8V, I_LOAD = 500 mA, L_DCR_max = 26 mΩ	-	84.8	-	
		VBAT = 4V, VOUT = 0.8V, I_LOAD = 1000mA, L_DCR_max = 26mΩ	-	84.1	-	
		VBAT = 4V, VOUT = 0.8V, I_LOAD = 2000mA, L_DCR_max = 26mΩ	-	76.5	-	
BUCK soft-start time	t_{SS_BUCK}	VOUT = 0.55V, I^2C programmable	110	-	1,000	µs
Switch frequency	f_{OSC_BUCK}	In FPWM	2.1	2.4	2.7	MHz
Output voltage ripple (PWM)		VBAT = 3.1V, I_LOAD = 0.5 x Imax 20 MHz measurement BW	-5.65% *Vo+11	-	+8%* Vo-11	mV
Output voltage ripple (PFM)		VBAT = 3.1V, I_LOAD = 0.5 x Imax 20MHz measurement BW	-5.65% *Vo+11	-	+8%* Vo-11	mV

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Load transient		VBAT = 3.1V, I_LOAD = 0.1 to 2.06A, tr/tf = 1 µs	-53	-	53	mV
Line transient		VIN = 5 to 4.3V/3.5V to 2.8V, Vout = 0.8V, I_LOAD = 2A	-40	-	40	mV
DC accuracy (includes line/load regulation@PWM)		VBAT = 3.1 to 5.0V I_LOAD = PWM load	-6	-	6	mV
DC accuracy (includes line/load regulation@PFM)		VBAT = 3.1 to 5.0V I_LOAD = PFM load	-10	-	22.5	mV
Output discharge switch on-resistance			-	11	-	Ω
BUCK1 supply current	I_{BUCK1_PVIN}	V_{BUCK1_PVIN} = 4V, I_{LOAD} = 0 mA, BUCK1_VOUT = 0.55V	-	4	6	µA
BUCK2						
Turn-on overshoot		VOUT = default, no load	-	-	10	%
Over-current protection (OCP)	I_{OCP2}	Peak inductor current, as REG_PMIC, 0x25[2:1] = 01	4	5	6	A
Efficiency	E_{ff_BUCK}	VBAT = 4V, Vout = 1.125V, I_LOAD = 100 mA, L_DCR_max = 26 mΩ	-	85	-	%
		VBAT = 4V, Vout = 1.125V, I_LOAD = 500 mA, L_DCR_max = 26 mΩ	-	83	-	
		VBAT = 4V, Vout = 1.125V, I_LOAD = 1,000 mA, L_DCR_max = 26 mΩ	-	78	-	
		VBAT = 4V, Vout = 1.125V, I_LOAD = 2,000 mA, L_DCR_max = 26 mΩ	-	69	-	
BUCK soft-start time	t_{SS_BUCK}	Vout = 1.125V I^2C programmable	-	-	1,000	µs
Switch frequency	f_{OSC_BUCK}	In FPWM	2.1	2.4	2.7	MHz
Output voltage ripple (PWM)		VBAT = 3.1V, Vout = 1.125V I_LOAD = 0 mA ~ Imax 20 MHz measurement BW	-	1	-	%
Output voltage ripple (PFM)		VBAT = 3.1V, Vout = 1.125V I_LOAD = 0 mA ~ Imax 20 MHz measurement BW	-	40	-	mVpp
Load transient		VBAT = 3.1V, Vout = 1.125V I_LOAD = 0.1~0.9A, tr/tf = 1 µs	-40	-	40	mV
Line transient		VIN = 5 ~ 4.3V/3.5V ~ 2.8V, Vout = 1.125V, I_LOAD = 2A	-40	-	40	mV
DC accuracy (includes line/load regulation@PWM)		VBAT = 3.1~5.0V I_LOAD = PWM load	-0.9	-	0.9	%
DC accuracy (includes line/load regulation@PFM)		VBAT = 3.1~5.0V I_LOAD = PFM load	-0.9	-	3	%
Output discharge switch on-resistance			-	11	-	Ω
BUCK2 supply current	I_{BUCK2_PVIN}	V_{BUCK2} = 4V, I_{LOAD} = 0 mA, BUCK2_VOUT = 1.125V	-	4	6	µA
LDO1 to 7 (LDO1: VFP/LDO2: VTP/LDO3: VMC/LDO5: VMCH/LDO6: VMDDR/LDO7: VDRAM2)						

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{LDO_VIN1}		max{Vo+ 0.35 ; 3.15}	-	5	V
	V_{LDO_VIN2}		max{Vo+ 0.35 ; 3.15}	-	5	
	V_{LDO_VIN3}	LDO7 = 1.8V/10 mA	2	-	5	
	V_{LDO_VIN3}	LDO6 = 0.75V/300 mA LDO7= 0.6V/600 mA	1.08	-	2	
Output voltage accuracy	ΔV_{OUT_LDO1}	V_{OUT} = 1.8V (default) I_{OUT} = 150 mA	-1	-	1	%
	ΔV_{OUT_LDO2}	V_{OUT} = 1.8V (default) I_{OUT} = 200 mA	-1	-	1	
	ΔV_{OUT_LDO3}	V_{OUT} = 3V (default) I_{OUT} = 200 mA	-1	-	1	
	ΔV_{OUT_LDO5}	V_{OUT} = 2.95V (default) I_{OUT} = 800 mA	-1	-	1	
	ΔV_{OUT_LDO6}	V_{OUT} = 0.75V (default) I_{OUT} = 300 mA	-1	-	1	
	ΔV_{OUT_LDO7}	V_{OUT} = 0.6V (default) I_{OUT} = 600 mA	-1	-	1	
Output current limit	I_{oc_LDO1}		225	-	420	mA
	I_{oc_LDO2}		300	-	560	
	I_{oc_LDO3}		300	-	500	
	I_{oc_LDO5}		1,200	-	2,000	
	I_{oc_LDO6}		450	-	840	
	I_{oc_LDO7}		900	-	1,680	
Output short current limit	$I_{SHORTLIM\_LDO1}$	OCFB_EN = 1	30	-	150	mA
	$I_{SHORTLIM\_LDO2}$	OCFB_EN = 1	40	-	200	
	$I_{SHORTLIM\_LDO3}$	OCFB_EN = 1	40	-	200	
	$I_{SHORTLIM\_LDO5}$	OCFB_EN = 1	160	-	800	
	$I_{SHORTLIM\_LDO6}$	OCFB_EN = 1	60	-	300	
	$I_{SHORTLIM\_LDO7}$	OCFB_EN = 1	120	-	600	
Dropout voltage	$V_{DROP\_LDO1/2/3/5}$	I_LOAD1 = 150 mA, I_LOAD2 = 200 mA, I_LOAD3 = 200 mA, I_LOAD5 = 800 mA	-	-	350	mV
	$V_{DROP\_LDO6/7}$	I_LOAD6 = 300 mA, I_LOAD7 = 600 mA	-	-	100	
Rated load current (I_rated)	I_{LDO1}	I_rated ≤ 150 mA	-	-	150	mA
	I_{LDO2}	I_rated ≤ 200 mA	-	-	200	
	I_{LDO3}	I_rated ≤ 200 mA	-	-	200	
	I_{LDO5}	I_rated ≤ 800 mA	-	-	800	
	I_{LDO6}	I_rated ≤ 300 mA	-	-	300	
	I_{LDO7}	I_rated ≤ 600 mA	-	-	600	
Power supply rejection ratio (PSRR)	$PSRR_{LDO1/2/3/5}$	1. I load ≤ I_rated 2. Freq = 50 Hz ~ 1kHz	-	45	-	dB
		1. I load ≤ I_rated 2. Freq = 1~10 kHz	-	30	-	
		1. I load ≤ I_rated 2. Freq = 10~100 kHz	-	15	-	

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
		1. I load ≤ I_rated 2. Freq = 100 kHz ~ 1 MHz	-	15	-	
	$PSRR_{LDO6/7}$	1. I load ≤ I_rated 2. Freq = 50 Hz ~ 1 kHz	-	75	-	
		1. I load ≤ I_rated 2. Freq = 1~10 kHz	-	55	-	
		1. I load ≤ I_rated 2. Freq = 10~100 kHz	-	40	-	
		1. I load ≤ I_rated 2. Freq = 100 kHz ~ 1 MHz	-	25	-	
Soft-start time	$t_{SS\_LDO1/2}$	V_{OUT_LDO} = 90% of V_{OUT_LDO} (target)	-	-	1,000	µs
	$t_{SS\_LDO3/5}$	V_{OUT_LDO} = 90% of V_{OUT_LDO} (target)	-	-	1,000	
	t_{SS_LDO6}	V_{OUT_LDO} = 90% of V_{OUT_LDO} (target)	-	-	2,000	
	t_{SS_LDO7}	V_{OUT_LDO} = 90% of V_{OUT_LDO} (target)	-	-	3,300	
Power off-time	$t_{off\_LDO1/2/3/7}$	V_{OUT_LDO} = 10% of V_{OUT_LDO} (target)	-	-	2,000	µs
	t_{off_LDO5}	V_{OUT_LDO} = 10% of V_{OUT_LDO} (target)	-	-	1,500	
	t_{off_LDO6}	V_{OUT_LDO} = 10% of V_{OUT_LDO} (target)	-	-	1,000	
Normal mode quiescent current	$I_{IQ\_NM\_LDO1/2/3/5}$	I_{LOAD} = 0 mA, LDO1/2/3 is from LDO_VIN1, LDO5 is from LDO_VIN2, not include base Iq.	-	-	32	µA
	$I_{IQ\_NM\_LDO6}$	I_{LOAD} = 0 mA, LDO6 is from LDO_VIN2 and LDO_VIN3, not include base Iq.	-	-	169	
	$I_{IQ\_NM\_LDO7}$	I_{LOAD} = 0 mA, LDO7 is from LDO_VIN2 and LDO_VIN3, not include base Iq.	-	-	143	
Low power mode quiescent current	$I_{IQ\_LP\_LDO1/2/3/5}$	I_{LOAD} = 0 mA, LDO1/2/3 is from LDO_VIN1, LDO5 is from LDO_VIN2, not include base Iq.	-	-	16	µA
	$I_{IQ\_LP\_LDO6}$	I_{LOAD} = 0 mA, LDO6 is from LDO_VIN2 and LDO_VIN3, not include base Iq.	-	-	20	
	$I_{IQ\_LP\_LDO7}$	I_{LOAD} = 0 mA, LDO7 is from LDO_VIN2 and LDO_VIN3, not include base Iq.	-	-	17.6	
I^2C characteristics						
LOW-level input voltage	$V_{IL\_I^2C}$		-	-	0.4	V
HIGH-level input voltage	$V_{IH\_I^2C}$		1.2	-	-	V
LOW-level output voltage	$V_{OL\_I^2C}$	Open-drain	-	-	0.4	V
Input current each I/O pin	$I_{IN\_I^2C}$	$0.1 \times V_{DD} < V_I < 0.9 \times V_{DD(MAX)}$	-10	-	10	µA
SCL clock frequency	$f_{SCL\_I^2C\_HSM}$	CB ≤ 100 pF	-	-	3.4	MHz
		100 pF ≤ CB ≤ 400 pF	-	-	1.7	
Data hold time	$t_{DH\_I^2C}$		30	-	-	ns
Data set-up time	$t_{DS\_I^2C}$		70	-	-	ns

(1) Note 1 A 10 kΩ NTC thermistor with β = 3,435K is suggested, and a SEMITEC 103KT1608T is in use.
(2) Note 2 Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0 mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.
(3) Note 3 Guaranteed by design.

3 Typical Operating Characteristics

3.1 Typical Operating Characteristics

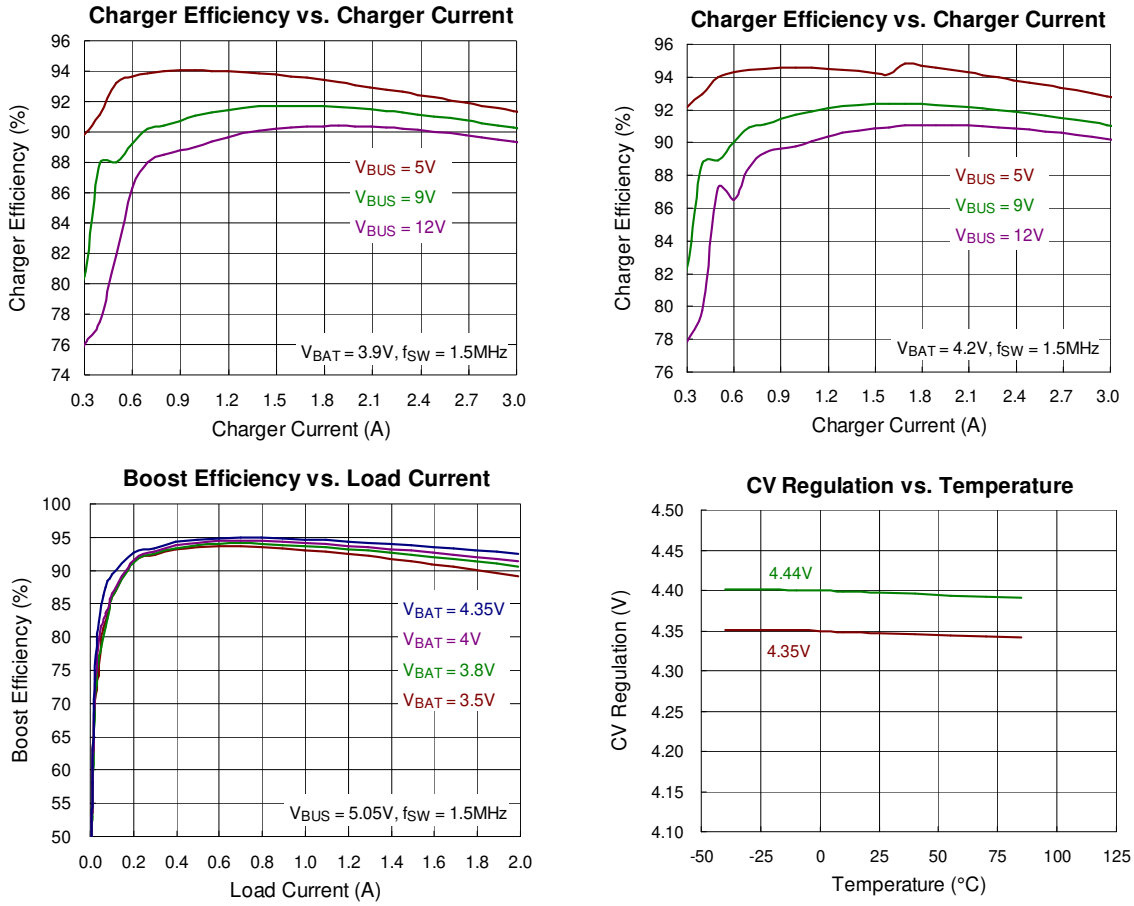
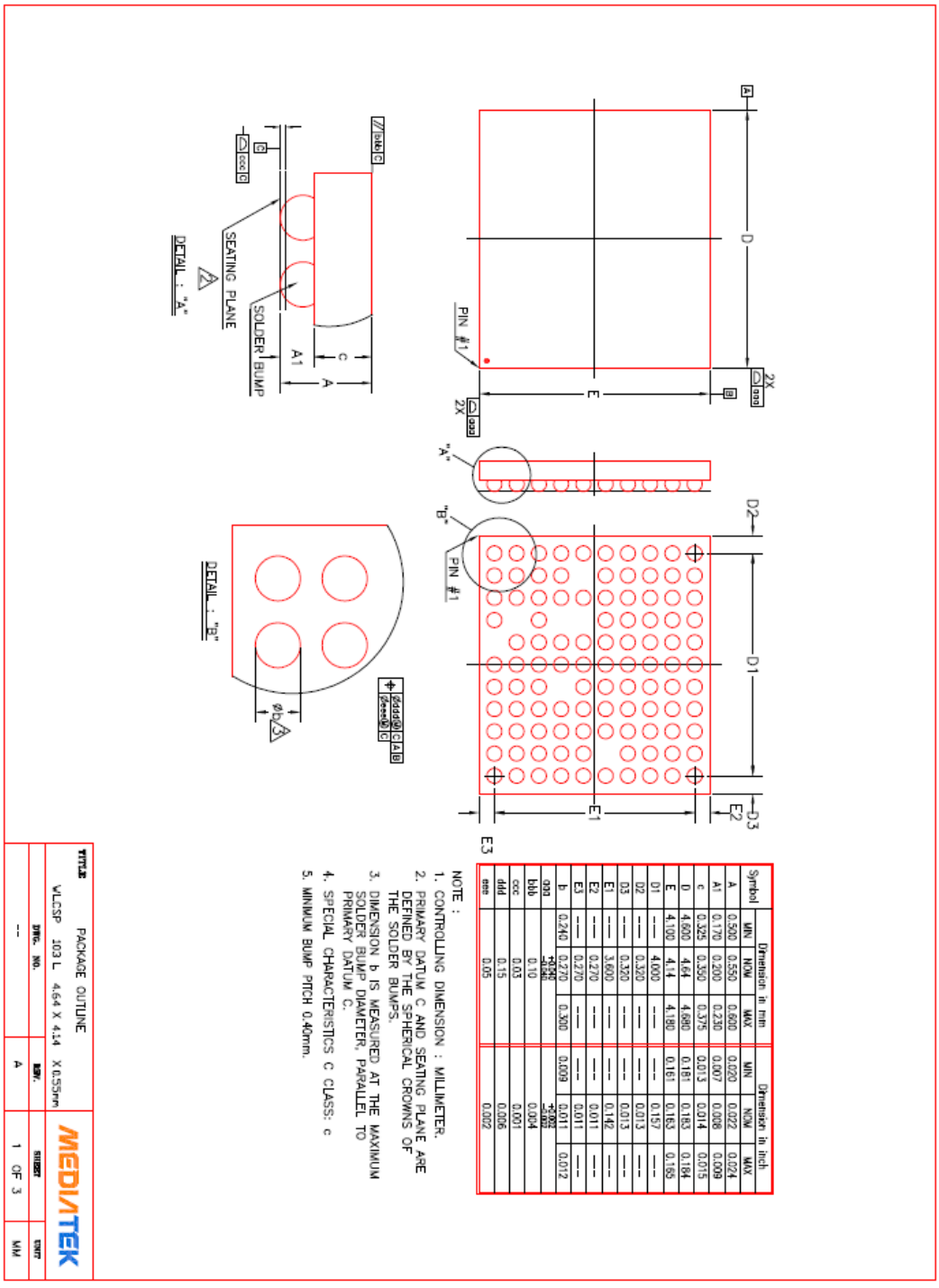


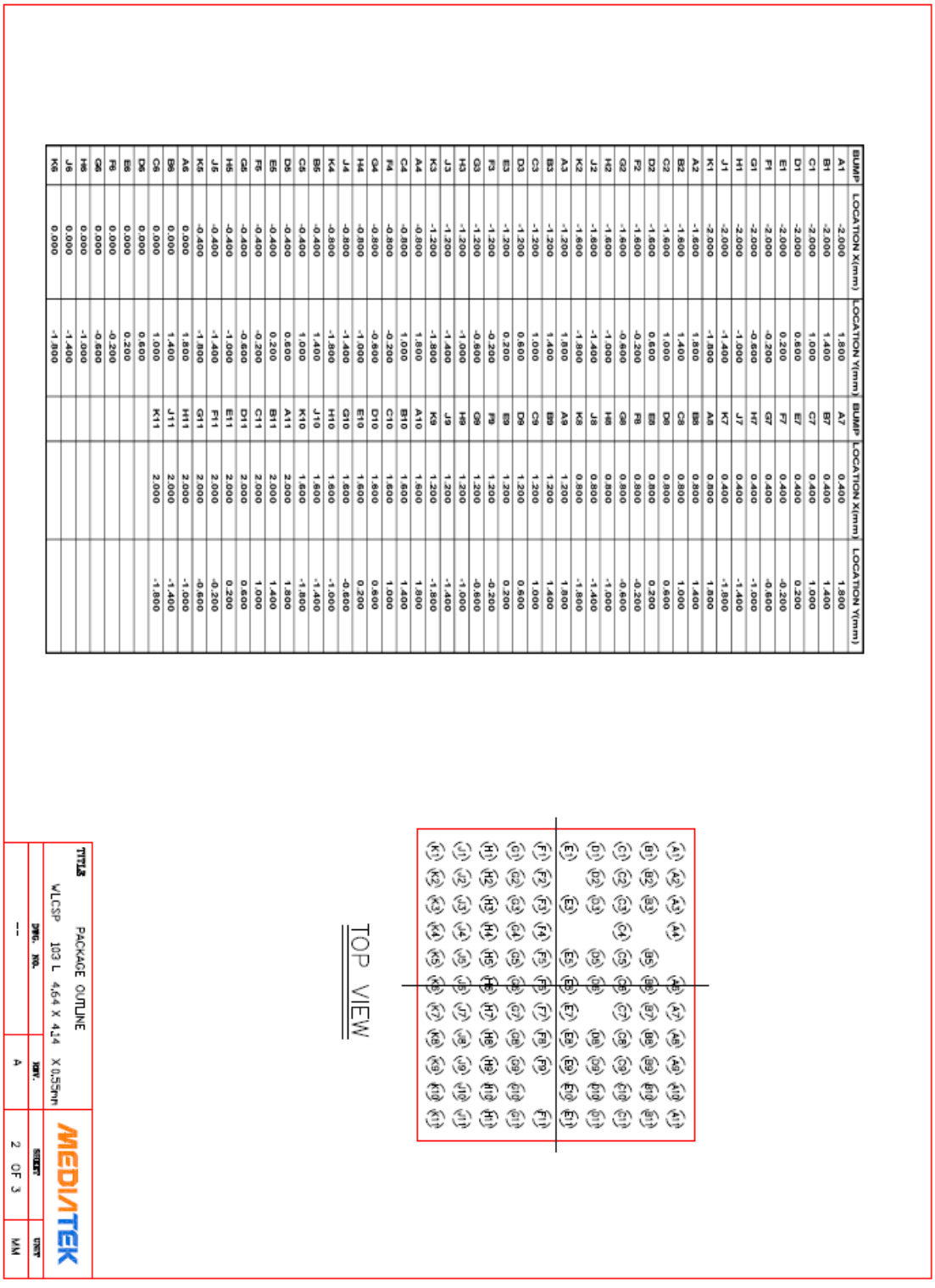
Figure 3-1. Typical operating characteristics

4 MT6360P Packaging

4.1 Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.500	0.550	0.600	0.020	0.022	0.024
A1	0.170	0.200	0.230	0.007	0.008	0.009
c	0.325	0.350	0.375	0.013	0.014	0.015
D	4.600	4.64	4.680	0.181	0.183	0.184
E	4.100	4.14	4.180	0.161	0.163	0.165
D1	----	4.000	----	----	0.157	----
D2	----	0.320	----	----	0.013	----
D3	----	0.320	----	----	0.013	----
E1	----	3.600	----	----	0.142	----
E2	----	0.270	----	----	0.011	----
E3	----	0.270	----	----	0.011	----
b	0.240	0.270	0.300	0.009	0.011	0.012
aaa		0.05			0.002	
bbb		0.10			0.004	
ccc		0.03			0.001	
ddd		0.15			0.006	
eee		0.05			0.002	



BUMP	LOCATION X(mm)	LOCATION Y(mm)	BUMP	LOCATION X(mm)	LOCATION Y(mm)
A1	-2.000	1.800	A7	0.400	1.800
B1	-2.000	1.400	B7	0.400	1.400
C1	-2.000	1.000	C7	0.400	1.000
D1	-2.000	0.600	E7	0.400	0.200
E1	-2.000	0.200	F7	0.400	-0.200
F1	-2.000	-0.200	G7	0.400	-0.600
G1	-2.000	-0.600	H7	0.400	-1.000
H1	-2.000	-1.000	J7	0.400	-1.400
J1	-2.000	-1.400	K7	0.400	-1.800
K1	-2.000	-1.800	A8	0.800	1.800
A2	-1.600	1.800	B8	0.800	1.400
B2	-1.600	1.400	C8	0.800	1.000
C2	-1.600	1.000	D8	0.800	0.600
D2	-1.600	0.600	E8	0.800	0.200
F2	-1.600	-0.200	F8	0.800	-0.200
G2	-1.600	-0.600	G8	0.800	-0.600
H2	-1.600	-1.000	H8	0.800	-1.000
J2	-1.600	-1.400	J8	0.800	-1.400
K2	-1.600	-1.800	K8	0.800	-1.800
A3	-1.200	1.800	A9	1.200	1.800
B3	-1.200	1.400	B9	1.200	1.400
C3	-1.200	1.000	C9	1.200	1.000
D3	-1.200	0.600	D9	1.200	0.600
E3	-1.200	0.200	E9	1.200	0.200
G3	-1.200	-0.600	G9	1.200	-0.600
H3	-1.200	-1.000	H9	1.200	-1.000
J3	-1.200	-1.400	J9	1.200	-1.400
K3	-1.200	-1.800	K9	1.200	-1.800
A4	-0.800	1.800	A10	1.600	1.800
C4	-0.800	1.000	B10	1.600	1.400
F4	-0.800	-0.200	C10	1.600	1.000
G4	-0.800	-0.600	D10	1.600	0.600
H4	-0.800	-1.000	E10	1.600	0.200
J4	-0.800	-1.400	G10	1.600	-0.600
K4	-0.800	-1.800	H10	1.600	-1.000
B5	-0.400	1.400	J10	1.600	-1.400
C5	-0.400	1.000	K10	1.600	-1.800
D5	-0.400	0.600	A11	2.000	1.800
E5	-0.400	0.200	B11	2.000	1.400
F5	-0.400	-0.200	C11	2.000	1.000
G5	-0.400	-0.600	D11	2.000	0.600
H5	-0.400	-1.000	E11	2.000	0.200
J5	-0.400	-1.400	F11	2.000	-0.200
K5	-0.400	-1.800	G11	2.000	-0.600
A6	0.000	1.800	H11	2.000	-1.000
B6	0.000	1.400	J11	2.000	-1.400
C6	0.000	1.000	K11	2.000	-1.800
D6	0.000	0.600			
E6	0.000	0.200			
F6	0.000	-0.200			
G6	0.000	-0.600			
H6	0.000	-1.000			
J6	0.000	-1.400			
K6	0.000	-1.800			

Figure 4-1. Package dimension

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