MT6319 Product Brief

Version: 1.0

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The full datasheet is available with an NDA

Version History

Version	Date	Description
1.0	2023-09-01	Official release

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1 Overview

1.1 Features

- Four high-efficiency step-down DC/DC
  - Max. output current 5A per phase
  - Phases bundled up to a 4-phase converter
  - Programmable over-current protection
  - Programmable loop compensation for each phase configuration by eFuse
  - Auto CCM/PFM, force-CCM operation and automatic low power mode setting
  - Remote differential feedback voltage sensing
  - Vout range = 0.3~1.19375V with 6.25 mV per step, DVS through compatible interface or SRCLKEN pin
- SPMI or I2C-compatible interface which supports high-speed modes in 5G modem application field
- Selectable interface (SPMI/I2C) by eFuse
- Dedicated FAULTB pin to report fault alarm to main PMIC
- Chip enable pin for on/off control
- Output short circuit and input over-voltage protection
- Over-temperature protection
- Input under-voltage lockout (UVLO)
- 45-pin 2.35×3.44 mm WLCSP package

1.2 Applications

- Smart phones, eBooks and tablets, mobile phones and Ultrabooks
- Handsets, gaming devices, car infotainment
- TV and media players
- Industrial HMI, desktop POS, KIOSK, digital signage

1.3 General Description

The MT6319 is designed to meet the power management requirements of the latest applications processors in mobile phones and similar portable applications.

The device contains four step-down DC/DC converters, which are bundled together in 4-phase buck converter and can be configured into various phase configurations by eFuse to power any application requirement.

The device is fully controlled by SPMI interface or an I2C compatible serial interface.

The MT6319 focuses on high-efficiency, step-down conversion over a wide output current range. The step-down converter enters the low power mode at light load for maximum efficiency. The regulator supports remote differential voltage sensing to compensate I*R drop between the regulator output and the load.

The protection features include short-circuit protection, output under voltage protection (power good function), input OVP, UVLO and temperature warning and shutdown functions.

Several fault flags are provided for status information of the IC.

During startup, the device controls the output slew rate to minimize output voltage overshoot and the inrush current.

The MT6319 is available in a 45-pin WLCSP package. The operating temperature ranges from -30°C to +85°C.

1.4 Ordering Information

Table 1-1. Ordering option

Order #	Marking	Temp. range	Package
MT6319LP/A		-30 ~ +85°C	WLCSP 45L

1.5 Part Voltage Table

Table 1-2. Part voltage table

Top marking (1)	Default voltage (V)	Imax (2) (mA)	Default on (Y/N)	Configuration	Lo	Application
MT6319LP/A	0.75	5,000*2	Y	VBUCK1	0.24 uH	CPUB
				VBUCK2	0.24 uH	
	1.125	5,000	Y	VBUCK3	0.24 uH	VDD2
	0.6	5,000	Y	VBUCK4	0.24 uH	VDDQ

(1) Note 1 The parts top marking (LP) interface is used by SPMI only.

(2) Note 2 Imax for multi-phase configurations should consider the over-temperature protection possibility since they are hosted in a tiny package.

1.6 Pin Assignment and Description

# 1	1	2	3	4	5	6	
A	PVDD2	VBUCK2	PGND2	PGND1	VBUCK1	PVDD1	A
B	PVDD2	VBUCK2	PGND2	PGND1	VBUCK1	PVDD1	B
C						INT	C
D	AV	VFBP2	VFBN2	FAULTB	VFBN1	VFBP1	D
E	DVDD18	FSOURCE	SRCLKEN	WDTRSTB	SCLK	SDAT	E
F	AG	VFBP4	VFBN4	EN	VFBN3	VFBP3	F
G	DVDD18_VIO					RSV1	G
H	PVDD4	VBUCK4	PGND4	PGND3	VBUCK3	PVDD3	H
J	PVDD4	VBUCK4	PGND4	PGND3	VBUCK3	PVDD3	J
	1	2	3	4	5	6	

Figure 1-1. MT6319 WLCSP 45L (2.35×3.44 mm) pin assignment

Table 1-3. MT6319 pin description

Ball	Symbol	I/O	Description
A5, B5	VBUCK1	O	Switching node for buck 1
A2, B2	VBUCK2	O	Switching node for buck 2
H5, J5	VBUCK3	O	Switching node for buck 3
H2, J2	VBUCK4	O	Switching node for buck 4
A6, B6	PVDD1	PWR	Power input for buck 1, to be connected to VSYS
A1, B1	PVDD2	PWR	Power input for buck 2, to be connected to VSYS
H6, J6	PVDD3	PWR	Power input for buck 3, to be connected to VSYS
H1, J1	PVDD4	PWR	Power input for buck 4, to be connected to VSYS
D1	AV	PWR	Analog input for buck, to be connected to VSYS
G1	DVDD18_VIO	PWR	Power to SPMI I/O, to make slave/master use the same power
A4, B4	PGND1	Power GND	Ground of power 1
A3, B3	PGND2	Power GND	Ground of power 2
H4, J4	PGND3	Power GND	Ground of power 3
H3, J3	PGND4	Power GND	Ground of power 4
F1	AG	Analog GND	Ground of analog
E1	DVDD18	PWR	Digital power 1.8V
D6	VFBP1	I	BUCK1 positive feedback
D5	VFBN1	I	BUCK1 negative ground feedback
D2	VFBP2	I	BUCK2 positive feedback
D3	VFBN2	I	BUCK2 negative ground feedback
F6	VFBP3	I	BUCK3 positive feedback
F5	VFBN3	I	BUCK3 negative ground feedback
F2	VFBP4	I	BUCK4 positive feedback
F3	VFBN4	I	BUCK4 negative ground feedback
F4	EN	I	Chip enable pin
E3	SRCLKEN	I	Sleep control input
E4	WDTRSTB	I	Watchdog reset input
E5	SCLK	IO	SPMI/I2C clock
E6	SDAT	IO	SPMI/I2C data
C6	INT	O	Interrupt output
D4	FAULTB	O	Fault alarm signal
E2	FSOURCE	I	eFuse power for programming
G6	RSV1	O	For analog test
C1~C5, G2~G5	NC		

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Condition	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery pin input (1)	Steady state	-0.5		6	V
	Transient (< 10 ms)	-0.5		6	V
Non-battery power pin (2)	Steady state	-0.5		5	V
Signal pin (3)	Steady state	-0.5		Vxx + 0.5 (3)	V
ESD robustness	HBM	2,000			V

(1) Note 1 VSYS_XXX/Vxxx (BUCK SW node)/VSYSSNS/BATADC -> battery input pin

(2) Note 2 Non-battery power input -> refer to Table 2-1 (PWR pin but not connected with battery)

(3) Note 3 Vxx = Max. operation voltage (refer to Table 2-2)

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Parameter	Condition	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient (Θ_{JA})	In free air		43.9		°C/W

Note. The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-7 condition.

2.3 Pin Voltage Range

The table below lists the operating voltage ranges for all MT6319 I/O pins.

Table 2-3. Pin voltage range

Ball	Symbol	Voltage range	Unit
A5, B5	VBUCK1	0~5	V
A2, B2	VBUCK2	0~5	V
H5, J5	VBUCK3	0~5	V
H2, J2	VBUCK4	0~5	V
A6, B6	PVDD1	0~5	V
A1, B1	PVDD2	0~5	V
H6, J6	PVDD3	0~5	V
H1, J1	PVDD4	0~5	V
D1	AV	0~5	V
G1	DVDD18_VIO	0~1.8	V
A4, B4	PGND1	0	V
A3, B3	PGND2	0	V
H4, J4	PGND3	0	V
H3, J3	PGND4	0	V
F1	AG	0	V
E1	DVDD18	0~1.8	V
D6	VFBP1	0~5	V
D5	VFBN1	0	V
D2	VFBP2	0~5	V
D3	VFBN2	0	V
F6	VFBP3	0~5	V
F5	VFBN3	0	V
F2	VFBP4	0~5	V
F3	VFBN4	0	V
F4	EN	0~5	V
E3	SRCLKEN	0~1.8	V
E4	WDTRSTB	0~1.8	V
E5	SCLK	0~1.8	V
E6	SDAT	0~1.8	V
C6	INT	0~1.8	V
D4	FAULTB	0~5	V
E2	FSOURCE	0~7.5	V
G6	RSV1	0~5	V

2.4 Recommended Operating Range

Table 2-4. Operation condition

Parameter	Condition	Min.	Typical	Max.	Unit
Operating temperature range		-30		85	°C

2.5 Electrical Characteristics

VBAT = 2.5~5V, minimum loads applied on all outputs, unless otherwise noted
Typical values are at TA = 25°C.

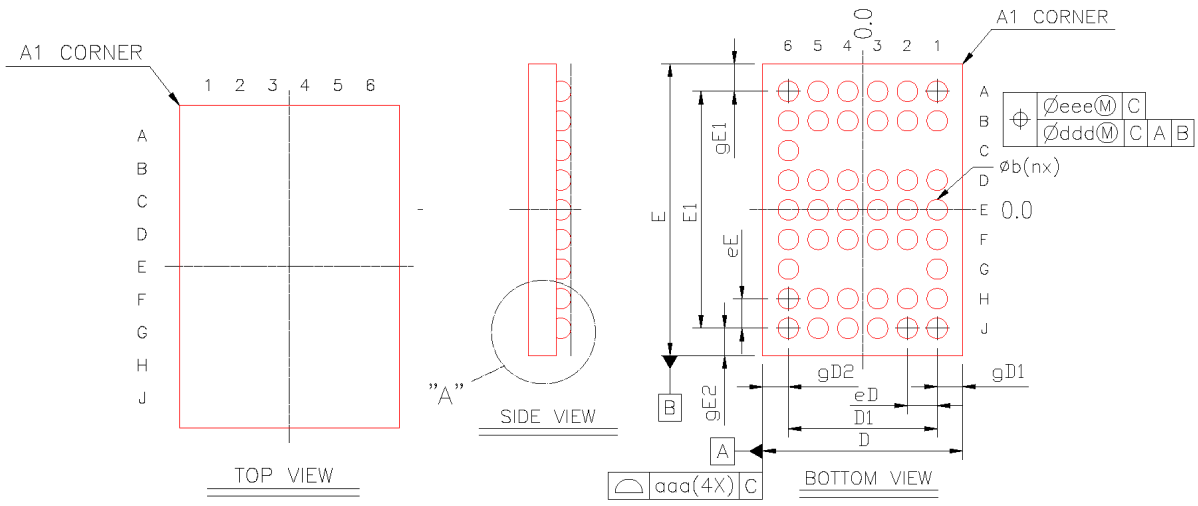
Table 2-5. General electrical specifications

Parameter	Condition	Min.	Typical	Max.	Unit
Operation ground current					
Standby (one buck on)	Low power mode Chip_EN = High Buck_EN = High		304.5	358	µA
Standby (all bucks off)	Low power mode Chip_EN = High Buck_EN = Low		13	17.5	µA
Off mode	Chip_EN = Low			1	µA
Under voltage (UV)					
Under voltage falling threshold			2.4		V
Under voltage rising threshold			2.65		V
Over voltage lockout (OVLO)					
Over voltage rising threshold		5.7	5.8	5.9	V
EN					
High voltage		1.41			V
Low voltage				0.9	V
Control input voltage (SCLK, SDAT, SRCLKEN related)					
Control input high		0.75*DVDD			V
Control input low				0.25*VIO	V
Thermal shutdown					
PMIC shutdown threshold			150		degree

3 MT6319 Packaging

3.1 Package Dimensions

Package: WLCSP 45L



Item		Symbol	Common Dimensions MIN.	NOM.	MAX
Package Type			WLCSP		
Body Size	X	D	2.3025	2.3525	2.3825
	Y	E	3.3949	3.4449	3.4749
Ball Pitch	X	eD	On-grid:0.3500 ref.		
	Y	eE	On-grid:0.3500 ref.		
Total Thickness		A	0.4600	0.5000	0.5400
Back Side Coating		A2	---		
Wafer Thickness		S	0.3050	0.3300	0.3550
Ball Diameter			0.2200		
Stand Off		A1	0.1400	0.1700	0.2000
Ball Width		b	0.2100	0.2400	0.2700
Package Edge Tolerance		aaa	+0.0300 −0.0500		
Coplanarity		ccc	0.0300		
Ball Offset (Package)		ddd	0.0500		
Ball Offset (Ball)		eee	0.0150		
Ball Count		n	45		
Edge Ball Center to Center	X	D1	1.7500		
	Y	E1	2.8000		
Edge Ball Center to Package Edge	X	gD1/gD2	0.30125		
	Y	gE1/gE2	0.32245		

Figure 3-1. Package dimensions

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